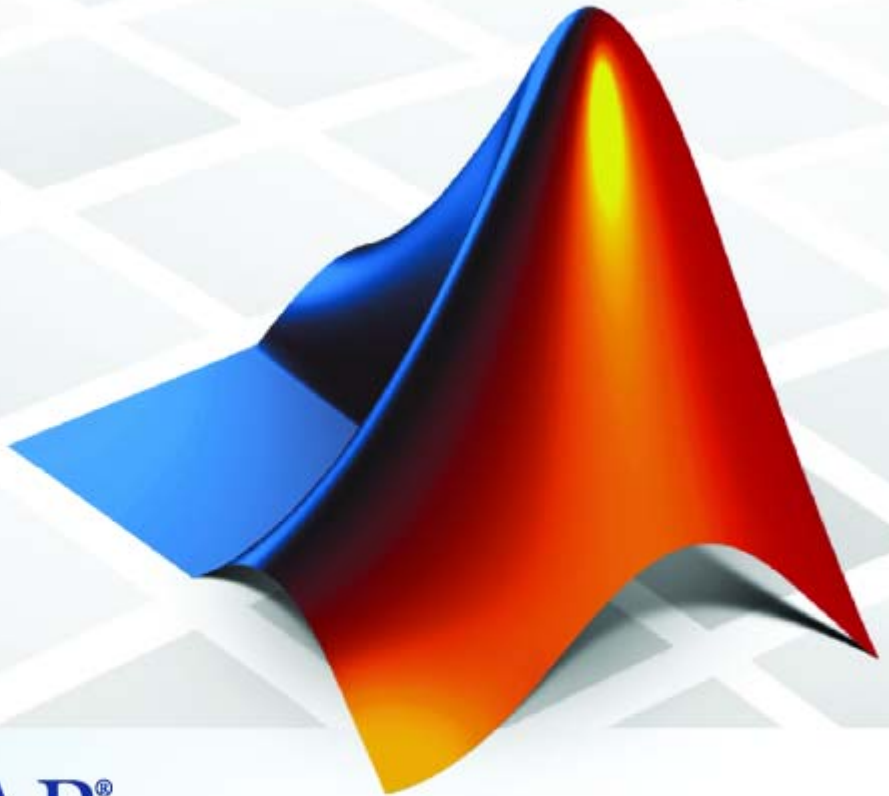


Link for Analog Devices VisualDSP++[®] 1 User's Guide



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Link for Analog Devices VisualDSP++ User's Guide

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Automation Interface

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Getting Started

What Is Link for VisualDSP++®?
(p. 1-2)

The Structure and Components
of Link for Analog Devices
VisualDSP++® (p. 1-4)

Introduces Link for Analog Devices
VisualDSP++®

Describes the two components
of Link for Analog Devices
VisualDSP++®

What Is Link for VisualDSP++®?

Link for VisualDSP++ provides a connection between MATLAB® and the VisualDSP++ IDDE to enable users to access the processor, manipulate data on the processor, and manage projects within the IDDE, while simultaneously utilizing the MATLAB tools of numerical analysis and simulation. Using Link for Analog Devices VisualDSP++® you can perform the following tasks, and others related to Model-Based Design:

- **Function calls** — Write scripts in MATLAB to execute any function in the VisualDSP++ IDDE
- **Automation** — Write automated tests in MATLAB to be executed on your processor, including control and verification operations
- **Host-Processor Communication** — Communicate with the processor directly from MATLAB, without going to the IDDE
- **Verification and Validation**
 - Load and execute projects into the VisualDSP++ IDDE from the MATLAB command line
 - Build and compile code, and then use vectors of test data and parameters to test the code
 - Build and compile your code, and then download the code to the processor and execute it
- **Design models** — Design models and algorithms in MATLAB and Simulink and run them on the processor
- **Generate code**— Generate executable code for your processor directly from the models designed in Simulink®, and execute it

Link for Analog Devices VisualDSP++® connects MATLAB® and Simulink® with VisualDSP++ integrated development and debugging environment from Analog Devices, Inc (ADI). Link for ADI VisualDSP++ enables you to use MATLAB and Simulink to debug and verify embedded code running on all Analog Devices DSPs that VisualDSP++ supports, such as the Blackfin, SHARC and TigerSHARC processor families.

Link for ADI VisualDSP++ includes a project generator component. With the project generator component, you can generate a complete project file for

VisualDSP++ from Simulink models, using C code generated with Real-Time Workshop®. Thus, you can use Real-Time Workshop and Real-Time Workshop Embedded Coder to generate generic ANSI C code projects for VisualDSP++ from Simulink models, that you can then build and run on Blackfin, SHARC, and TigerSHARC processors.

The following list suggests some of the uses for Link for ADI VisualDSP++:

- Create test benches in MATLAB and Simulink for testing your hand written or automatically generated code running on ADI DSPs
- Generate code and project files for VisualDSP++ from Simulink models using Real-Time Workshop and Real-Time Workshop Embedded Coder for rapid prototyping or deployment of a system or application
- Build, debug, and verify embedded code on ADI DSPs with MATLAB, Simulink, and VisualDSP++
- Perform processor-in-the-loop (PIL) testing of embedded code

The Structure and Components of Link for Analog Devices VisualDSP++®

In this section...
“Automation Interface” on page 1-4
“Project Generator” on page 1-5
“Verification” on page 1-5

Link for Analog Devices VisualDSP++® comprises components—the Automation Interface component, the Project Generation component, and the Verification component. The Automation Interface component enables communication between MATLAB and Link for Analog Devices VisualDSP++®. It is built on MATLAB alone. The Project Generation component is built on SIMULINK and lets you build models, simulate them, and generate code from the models directly to the processor.

The Verification component offers capabilities that help you use Model-Based Design to validate and verify your projects. With the Verification component, you can simulate algorithms and processes in Simulink models and concurrently on your processor. Comparing the results helps verify the fidelity of your model or algorithm code.

Automation Interface

The Automation Interface component allows users to use MATLAB functions and methods to communicate with the VisualDSP++ IDDE to automate project management, to debug, to manipulate the data in the processor memory (internal and external) and registers, and to exercise functions from your project on the processor, and to communicate between the host and processor applications. The functionality provided by the automation interface component can be divided into the following categories:

- Debug Component — Methods and functions for project automation, debugging, and data manipulation.
- Function Call Component — Methods that allow the you to invoke individual functions on the processor.

- Host Processor Communication Component — Methods that support various standard communication protocols, such as BTC, TCP/IP, and UDP.

Project Generator

The Project Generator component is a collection of methods that utilize the VisualDSP++ API to create projects in VisualDSP++ and generate code with Real-Time Workshop®. With the interface, you can do the following:

- Automatic project-based build process — Automatically create and build projects for code generated by Real-Time Workshop or Real-Time Workshop Embedded Coder.
- Custom code generation — Use Link for ADI VisualDSP++ with any Real-Time Workshop System Target File (STF) to generate processor-specific and optimized code.
- Automatic downloading and debugging — Debug generated code in the VisualDSP++ debugger, using either the instruction set simulator or real hardware.
- Create and build projects for VisualDSP++ from Simulink models — Project Generator uses Real-Time Workshop or Real-Time Workshop Embedded Coder to build projects that work with Analog Devices processors.
- Generate custom code using the Configuration Parameters in your model with the system target files `vdsplink_ert.tlc` and `vdsplink_grt.tlc`.

Verification

Verifying your processes and algorithms is an essential part of developing applications. The components of Link for ADI VisualDSP++ combine to provide the following verification tools for you to apply as you develop your code:

Processor-in-the-Loop Cosimulation

Use cosimulation techniques to verify generated code running in an instruction set simulator or real hardware environment.

Execution Profiling

Gather execution profiling measurements with VisualDSP++ instruction set simulator to establish the timing requirements of your algorithm.

Automation Interface

Getting Started with Automation Interface (p. 2-2)

Guides you through the process of creating and using objects and embedded objects

Constructing Objects (p. 2-13)

Explains what an adivdsp object is and how to construct one

Properties and Property Values (p. 2-15)

Describes how to work with objects, their properties and property values

adivdsp Object Properties (p. 2-19)

Describes the properties of link objects

Getting Started with Automation Interface

In this section...
“Introducing the Link for ADI VisualDSP++ Tutorial” on page 2-2
“Running the Interactive Tutorial” on page 2-5
“Selecting Your Session and Processor” on page 2-5
“Querying Objects for VisualDSP++” on page 2-6
“Loading Files into VisualDSP++” on page 2-8
“Running the Project” on page 2-10
“Closing the Connections or Cleaning Up VisualDSP++” on page 2-11

Link for ADI VisualDSP++ provides a connection between MATLAB and a processor in VisualDSP++. You can use objects as a mechanism to control and manipulate a signal processing application using the computational power of MATLAB. This approach can help you while you debug and develop your application. Another possible use for automation is creating MATLAB scripts that verify and test algorithms that run in their final implementation on your production processor.

Note Before using the functions available with the objects, you must select a session in VisualDSP++. The object you create is specific to a designated session in VisualDSP++ IDDE.

Introducing the Link for ADI VisualDSP++ Tutorial

To get you started using objects for VisualDSP++ IDDE software, Link for ADI VisualDSP++ includes an example script `vdsp tutorial.m`. As you work through this tutorial, you perform the following tasks that step you through creating and using objects for VisualDSP++ IDDE:

- 1 Select your session.
- 2 Create and query objects to VisualDSP++ IDDE.
- 3 Use MATLAB to load files into VisualDSP++ IDDE.

- 4 Work with your VisualDSP++ IDDE project from MATLAB.
- 5 Close the connections you opened to VisualDSP++ IDDE.

The tutorial covers some methods and functions for Link for ADI VisualDSP++. The functions listed first do not require an object. The functions listed after that require an existing `adivdsp` object before you can use the function syntax.

Functions for Working with VisualDSP++

The following table shows functions that do not require an object.

Function	Description
<code>listsessions</code>	Return information about the boards that VisualDSP++ IDDE recognizes as installed on your PC.
<code>adivdsp</code>	Construct an object that refers to a VisualDSP++ IDDE session. When you construct the object you specify the session by processor.

Methods for Working with `adivdsp` Objects in VisualDSP++

The following table presents some of the methods that require an `adivdsp` object.

Methods	Description
<code>add</code>	Add a file to a project
<code>address</code>	Return the address and page for an entry in the symbol table in VisualDSP++ IDDE
<code>build</code>	Build the project in VisualDSP++
<code>cd</code>	Change the working directory
<code>display</code>	Display the properties of an object that references a VisualDSP++ session
<code>halt</code>	Terminate execution of a process running on the processor

Methods	Description
info	Return information about the object or session
isrunning	Test whether the processor is executing a process
load	Load a built project to the processor
open	Open a file in the project
read	Retrieve data from memory on the processor
reset	Restore the program counter (PC) to the entry point for the current program
run	Execute the program loaded on the processor
save	Save files or projects
visible	Set whether VisualDSP++ IDDE window is visible on the desktop while VisualDSP++ IDDE is running
write	Write data to memory on the processor

Running VisualDSP++ on Your Desktop – Visibility

When you create an `adivdsp` object in the tutorial in the next section, Link for ADI VisualDSP++ starts VisualDSP++ in the background.

If VisualDSP++ is running in the background, it does not appear on your desktop, in your task bar, or on the **Applications** page in the Task Manager. It does appear as a process, `idde.exe`, on the **Processes** tab in Task Manager.

You can make the VisualDSP++ IDE visible with the function `visible`. The function `isvisible` returns the status of the IDE—is it visible on your desktop. To close the IDDE when it is not visible and MATLAB is not running, use the **Processes** tab in Windows Task Manager and look for `idde.exe`.

If an object that refers to VisualDSP++ exists when you close VisualDSP++, the application does not close. Windows moves it to the background (it becomes invisible). Only after you clear all objects that access VisualDSP++, or close MATLAB, does closing VisualDSP++ unload the application. You can see if VisualDSP++ is running in the background by checking in the Windows

Task Manager. When VisualDSP++ is running, the entry `idde.exe` appears in the **Image Name** list on the **Processes** tab.

Running the Interactive Tutorial

You have the option of running this tutorial from the MATLAB command line or entering the functions as described in the following tutorial sections.

To run the tutorial in MATLAB, click `run vdspautointtutorial`. This command launches the tutorial in an interactive mode where the tutorial program provides prompts and text descriptions to which you respond to move to the next section. The interactive tutorial covers the same information provided by the following tutorial sections. You can view the tutorial M-file used here by clicking `vdspautointtutorial.m`.

Note To run the interactive tutorial, you must have at least one session configured in VisualDSP++. If you do not yet have a session, use the Analog Devices VisualDSP++ Configurator to create a session to use for this tutorial.

Selecting Your Session and Processor

Link for ADI VisualDSP++ IDDE requires that you have at least one session available for VisualDSP++. To help you select the session to use for this tutorial, and for any development work, Link for ADI VisualDSP++ provides a command line tool, called `listsessions`, which prints a list of the available sessions. So that you can use this function in a script, `listsessions` can return a MATLAB structure that you use when you want your script to select a session in the IDDE without your help.

Note The session you select is used throughout the tutorial.

- 1 To see a list of the sessions that you can use, enter the following command at the MATLAB prompt:

```
session_list = listsessions
```

MATLAB returns a list that shows all the sessions that Link for ADI VisualDSP++ IDDE recognizes as available in your installation.

```
session_list =  
  
    'ADSP-21060 ADSP-2106x Simulator'  
    'ADSP-21362 ADSP-2136x Simulator'
```

2 Use `adivdsp` to create an object that accesses a session in VisualDSP++.

```
vd = adivdsp('sessionname', 'ADSP-21362 ADSP-2136x Simulator', 'procnum', 0)
```

`Sessionname` and `procnum` are property names that specify the property to set. `ADSP-21362 ADSP-2136x Simulator` is the session to access, and 0 is the number of the processor to refer to in the session.

When you use `adivdsp`, you create an object, in this case `vd`, that refers to the session you specify in `sessionname`.

Querying Objects for VisualDSP++

In this tutorial section you create the connection between MATLAB and VisualDSP++ IDDE. This connection, or object, is a MATLAB object, which for this session you save as variable `vd`. You use function `adivdsp` to create objects. When you create objects, `adivdsp` input arguments let you define other object properties, such as the global time-out. Refer to the `adivdsp` reference information for more about the input arguments.

Use the generated object `vd` to direct actions to your session processor. In the following tasks, `vd` appears in all function syntax that interact with IDDE session and the processor: The object `vd` identifies and refers to a specific session. You need to include the object in any method syntax you use to access and manipulate a project or files in a session in VisualDSP++.

1 Create an object that refers to your selected session and processor. Enter the following command at the prompt.

```
vd = adivdsp('sessionname', 'ADSP-21362 ADSP-2136x Simulator', 'procnum', 0)
```

If you watch closely, and your machine is not too fast, you see VisualDSP++ appear briefly when you call `adivdsp`. If VisualDSP++ was not running

before you created the new object, VisualDSP++ launches and runs in the background.

Usually, you need to interact with VisualDSP++ while you develop your application. The function `visible`, controls the state of VisualDSP++ on your desktop. `visible` accepts Boolean inputs that make VisualDSP++ either visible on your desktop (input to `visible` ≥ 1) or invisible on your desktop (input to `visible` = 0). For this tutorial, you need to interact with the development environment, so use `visible` to set the IDDE visibility to 1.

- 2 To make VisualDSP++ show on your desktop, enter the following command at the command prompt:

```
visible(vd,1)
```

- 3 Next, enter `display(vd)` at the prompt to see the status information.

```
ADIVDSP Object:
  Session name      : ADSP-21362 ADSP-2136x Simulator
  Processor name    : ADSP-21362
  Processor type    : ADSP-21362
  Processor number  : 0
  Default timeout   : 10.00 secs
```

Link for ADI VisualDSP++ provides three methods to read the status of a processor:

- `info` — Return a structure of testable session conditions.
- `display` — Print information about the session and processor.
- `isrunning` — Return the state (running or halted) of the processor.

- 4 Type `linkinfo = info(vd)`.

The `vd` link status information provides data about the hardware, as follows:

```
linkinfo =
  procname: 'ADSP-21362'
  proctype: 'ADSP-21362'
```

```
revision: ''
```

5 Verify that the processor is running by entering

```
runstatus = isrunning(vd)
```

MATLAB responds, indicating that the processor is stopped, as follows:

```
runstatus =
```

```
0
```

Loading Files into VisualDSP++

You have established the connection to a processor and board. Using three methods you learned about the hardware, whether it was running, its type, and whether VisualDSP++ IDDE was visible. Next, give the processor something to do.

In this part of the tutorial, you load the executable code for the CPU in the IDDE. Link for ADI VisualDSP++ includes a tutorial project file for VisualDSP++. Through the next commands in the tutorial, you locate the tutorial project file and load it into VisualDSP++. The open method directs VisualDSP++ to load a project file or workspace file.

Note To continue the tutorial, you must identify or create a directory to which you have write access. Link for ADI VisualDSP++ cannot create a directory for you. If you do not have a writable directory, create one in Windows before you proceed with the rest of this tutorial.

VisualDSP++ has its own workspace and workspace files that are quite different from MATLAB workspace files and the MATLAB workspace. Remember to monitor both workspaces. The next steps change the working directory to your new writable directory.

1 Use `cd` to switch to the writable directory

```
prj_dir=cd('C:\vdsp_demo')
```


where the name and path to the writable directory is a string, such as `C:\vdsp_demo` as used in the example. Replace `C:\vdsp_demo` with the full path to your directory.

- 2 Change your working directory to the new directory by entering the following command:

```
cd(vd,prj_dir)
```

- 3 Next, use the following command to create a new VisualDSP++ project named `dot_product_c.dpj` in the new directory:

```
new(vd,'dot_product_c.dpj')
```

Look in the IDDE to verify that your new project exists. Next you need to add source files to your project.

- 4 Add the two provided source files, `—dotprod.c` and `dotprod_main.c` to the project `dot_product_c.dpj` using the following two commands:

```
add(vd,'matlabroot\toolbox\vdsp\link\vdspdemos\src\dotprod.c')
add(vd,'matlabroot\toolbox\vdsp\link\vdspdemos\src\dotprod_main.c')
```

The variable `matlabroot` indicates the root directory of your MATLAB installation. Replace `matlabroot` with the path to MATLAB on your machine. For more information about the MATLAB root directory, refer to `matlabroot` in the MATLAB documentation.

- 5 Open the files in the IDDE from MATLAB by issuing the following commands to open each file separately:

```
open(vd,'matlabroot\toolbox\vdsp\link\vdspdemos\src\dotprod.c')
open(vd,'matlabroot\toolbox\vdsp\link\vdspdemos\src\dotprod_main.c')
```

Switch to the IDDE to verify that the files are in your project and open.

- 6 Save your project.

```
save(vd,'dot_product_c.dpj','project')
```

Your IDDE project is saved with the name `dot_product_c.dpj` in your writable directory. The input string 'project' specifies that you are saving a project file.

Running the Project

After you create `dot_project_c.dpj` in the IDDE, you can use Link for ADI VisualDSP++ functions to create executable code from the project and load the code to the processor.

The next steps in this tutorial build the executable and download and run it on your processor.

- 1 Use the following build command to build an executable module from the project `dot_product_c.dpj`.

```
build(vd,30) % The optional input argument 30 sets the time out period to 30 seconds.
```

At the end of the build process, Link for ADI VisualDSP++ returns a value of 1 to indicate that the build succeeded. If the build process returns a 0, the build failed.

```
ans =
```

```
1
```

- 2 To load the new executable to the processor, use `load` with the project file name and the object name. The name of the executable is `dot_product_c.dxe`, and it is stored with the project in your writable directory, in a subdirectory named `debug`.

```
load(vd, 'c:\vdsp_demo\debug\dot_product_c.dxe', 30);
```

Link for ADI VisualDSP++ provides methods to control processor execution—`run`, `halt`, and `reset`. To demonstrate these methods, use `run` to start the program you just loaded on to the processor, and then use `halt` to stop the processor.

- 1 Try the following methods at the command prompt.

```
run(vd)      % Start the program running on the processor.  
halt(vd)     % Halt the processor.  
reset(vd)    % Reset the program counter to start of program.
```

Use `isrunning` after the `run` method to verify that the processor is running. After you stop the processor, `isrunning` can verify that the processor has stopped.

Closing the Connections or Cleaning Up VisualDSP++

Objects that you create in Link for ADI VisualDSP++ have connections to VisualDSP++. Until you delete these handles, the VisualDSP++ process (`idde.exe` in the Windows Task Manager) remains in memory. Closing MATLAB removes these objects automatically, but there may be times when it helps to delete the handles manually, without quitting MATLAB.

Note When you clear the last `adivdsp` object, Link for ADI VisualDSP++ closes VisualDSP++. When it closes the IDDE, it does not save current projects or files in the IDDE, and it does not prompt you to save them. A best practice is to save all of your projects and files before you clear `adivdsp` objects from your MATLAB workspace.

Use the following command to close the project files in VisualDSP++.

```
close(vd, 'all', 'text')
```

Finally, to delete your link to VisualDSP++ use `clear vd`.

You have completed the Automation Interface tutorial using Link for Analog Devices VisualDSP++.

During the tutorial you performed the following tasks:

- 1 Selected your session.
- 2 Created and queried objects that refer to a session in Link for Analog Devices VisualDSP++ to get information about the session and processor.
- 3 Used MATLAB to load files into VisualDSP++, and used methods in MATLAB to run that file.
- 4 Closed the links you opened to VisualDSP++.

This set of tasks is used In any development work you do with signal processing applications. Thus, the tutorial provided here gives you a working process for using Link for ADI VisualDSP++ and your signal processing programs to develop programs for a range of Analog Devices processors.

Constructing Objects

When you create a connection to a session in VisualDSP++ using the `adivdsp` function, you create an object. The object implementation relies on MATLAB object-oriented programming capabilities similar to the objects you find in MATLAB or Filter Design Toolbox.

The discussions in this section apply to the objects in Link for ADI VisualDSP++. Because `adivdsp` objects use the MATLAB programming techniques, the information about working with the objects, such as how you get or set properties, or use methods, apply to the objects you create in Link for ADI VisualDSP++.

Like other MATLAB structures, objects in Link for Analog Devices VisualDSP++ have predefined fields referred to as *object properties*.

You specify object property values by one of the following methods:

- Specifying the property values when you create the object
- Creating an object with default property values, and changing some or all of these property values later

For examples of setting link properties, refer to “Setting Property Values with `set`”.

Example – Constructor for `adivdsp` Objects

The easiest way to create an object is to use the function `adivdsp` to create an object with the default properties. Create an object named `vd` referring to a session in VisualDSP++ by entering the following syntax:

```
vd = adivdsp
```

MATLAB responds with a list of the properties of the object `vd` you created along with the associated default property values.

```
ADIVDSP Object:
  Session name      : ADSP-21362 ADSP-2136x Simulator
  Processor name    : ADSP-21362
  Processor type    : ADSP-21362
```

Processor number : 0
Default timeout : 10.00 secs

The object properties are described in the `adivdsp` documentation.

Note These properties are set to default values when you construct links.

Properties and Property Values

In this section...

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“Setting Property Values Directly at Construction” on page 2-16

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“Direct Property Referencing to Set and Get Values” on page 2-17

“Overloaded Functions for adivdsp Objects” on page 2-18

Links (or objects) in this Link for ADI VisualDSP++ have properties associated with them. Each property is assigned a value. You can set the values of most properties, either when you create the link or by changing the property value later. However, some properties have read-only values. Also, a few property values, such as the board number and the processor to which the link attaches, become read-only after you create the object. You cannot change those after you create your link.

Setting and Retrieving Property Values

You can set Link for ADI VisualDSP++ for Analog Devices DSP link property values by either of the following methods:

- Directly when you create the link — see “Setting Property Values Directly at Construction”
- By using the set function with an existing link — see “Setting Property Values with set”

Retrieve Link for Analog Devices VisualDSP++ object property values with the get function.

Direct property referencing lets you either set or retrieve property values for adivdsp objects.

Setting Property Values Directly at Construction

To set property values directly when you construct an object, include the following entries in the input argument list for the constructor method `adivdsp`:

- A string for the property name to set followed by a comma. Enclose the string in single quotation marks as you do any string in MATLAB.
- The associated property value. Sometimes this value is also a string.

Include as many property names in the argument list for the object construction command as there are properties to set directly.

Example — Setting Link Property Values at Construction

Suppose that you want to create a link to a session in VisualDSP++ and set the following object properties:

- Link to the specified session.
- Connect to the first processor.
- Set the global time-out to 5 s. The default is 10 s.

Set these properties by entering

```
vd = adivdsp('sessionname','ADSP-21060 ADSP-2106x Simulator','procnum',0,'timeout',5);
```

The `sessionname`, `procnum`, and `timeout` properties are described in [Link Properties](#), as are the other properties for links.

Setting Property Values with `set`

After you construct an object, the `set` function lets you modify its property values.

Using the `set` function, you can change the value of any writable property of an object.

Example — Setting Link Property Values Using `set`

To set the time-out specification for the link `vd` from the previous section, enter the following syntax:

```
set(vd,'timeout',8);

get(vd,'timeout');
ans=

     8
```

The display reflects the changes in the property values.

Retrieving Properties with `get`

You can use the `get` command to retrieve the value of an object property.

Example — Retrieving Link Property Values Using `get`

To retrieve the value of the `sessionname` property for `vd2`, and assign it to a variable, enter the following syntax:

```
session=get(vd2,'sessionname')

session =

ADSP-21060 ADSP-2106x Simulator
```

Direct Property Referencing to Set and Get Values

You can directly set or get property values using MATLAB structure-like referencing. Do this by using a period to access an object property by name, as shown in the following example.

Example — Direct Property Referencing in Links

To reference an object property value directly, perform the following steps:

- 1 Create a link with default values.
- 2 Change its time-out and number of open channels.

```
vd = adivdsp;  
vd.time = 6;
```

Overloaded Functions for adivdsp Objects

Several methods and functions in Link for ADI VisualDSP++ have the same name as functions in other MathWorks products. These functions behave similarly to their original counterparts, but you apply them to an object. This concept of having functions with the same name operate on different types of objects (or on data) is called *overloading* of functions.

For example, the `set` command is overloaded for objects. After you specify your object by assigning values to its properties, you can apply the methods in this toolbox (such as `address` for reading an address in memory) directly to the variable name you assign to your object. You do not have to specify your object parameters again.

For a complete list of the methods that act on `adivdsp` objects, refer to the Chapter 6, “Functions — Alphabetical List” in the function reference pages.

adivdsp Object Properties

In this section...

“Quick Reference to adivdsp Properties” on page 2-19

“Details About adivdsp Object Properties” on page 2-20

Link for ADI VisualDSP++ provides links to your processor hardware so you can communicate with processors for which you are developing systems and algorithms. Because Link for ADI VisualDSP++ uses objects to create the links, the parameters you set are called properties and you treat them as properties when you set them, retrieve them, or modify them.

This section details the properties for the objects for VisualDSP++. First the section provides tables of the properties, for quick reference. Following the tables, the section offers in-depth descriptions of each property, its name and use, and whether you can set and get the property value associated with the property. Descriptions include a few examples of the property in use.

MATLAB users may find much of this handling of objects familiar. Objects in Link for ADI VisualDSP++ behave like objects in MATLAB and the other object-oriented toolbox products. C++ programmers may already understand the concepts described in this section.

Quick Reference to adivdsp Properties

The following table lists the properties for the links in Link for ADI VisualDSP++. The second column indicates to which object the property belongs. Knowing which property belongs to each object in a link tells you how to access the property.

Property Name	User Settable?	Description
sessionname	At construction only	Reports the name of the session in VisualDSP++ that the object references.

Property Name	User Settable?	Description
procnum	At construction only	Stores the number of the processor in the session. If you have more than one processor, this number identifies the specific processor.
timeout	Yes/default	Contains the global time-out setting for the link.

Some properties are read only. Thus, you cannot set the property value. Other properties you can change at any time. If the entry in the User Settable column is “At construction only”, you can set the property value only when you create the object. Thereafter it is read only.

Details About adivdsp Object Properties

To use the objects for VisualDSP++ interface, set values for the following:

- `sessionname` — Specify the session with which the object interacts.
- `procnum` — Specify the processor in the session. If the board has multiple processors, `procnum` identifies the processor to use.
- `timeout` — Specify the global time-out value. (Optional. Default is 10 s.)

Details of the properties associated with `adivdsp` objects appear in the following sections, listed in alphabetical order by property name.

procnum

Property `procnum` identifies the processor referenced by an object for Link for Analog Devices VisualDSP++ IDDE. Use `procnum` to specify the processor you are working with in the session specified by `sessionname`. The VisualDSP++ Configurator assigns a number to each processor installed in each session. To determine the value of `procnum` for a processor, use `listsessions` or the Configurator.

To identify a processor, you need the `sessionname` and `procnum` values. For sessions with one processor, `procnum` equals 0. VisualDSP++ IDDE numbers the processors on multiprocessor boards sequentially from 0 to the total

number of processors. For example, on a board with four processors, the processors are numbered 0, 1, 2, and 3.

sessionname

Property `sessionname` identifies the session referenced by a Link for Analog Devices VisualDSP++. When you create an object, you use `sessionname` to specify the session you are intending to interact with. To get the value for `sessionname`, use `listsessions` or the Analog Devices VisualDSP++ Configurator. The Configurator utility assigns the name for each session available on your system.

timeout

Property `timeout` specifies how long VisualDSP++ waits for any process to finish. You set the global time-out when you create an object for a session in VisualDSP++. The default global time-out value is 10 s. The following example shows the `timeout` value for object `vd2`.

```
display(vd2)
```

```
ADIVDSP Object:
```

```
Session name      : ADSP-21060 ADSP-2106x Simulator
Processor name    : ADSP-21060
Processor type    : ADSP-21060
Processor number  : 0
Default timeout   : 10.00 secs
```


Project Generator

Introducing Project Generator (p. 3-2)	Describes code generation with Project Generator
Using the Link for Analog Devices VisualDSP++ Blockset (p. 3-3)	Describes the contents of the vdsplinklib blockset
Schedulers and Timing (p. 3-10)	Describes the timer-based and asynchronous schedulers
Project Generator Tutorial (p. 3-17)	Takes you through the process of creating models in Simulink and generating code for your processors.
Setting Real-Time Workshop Options for Analog Devices Processors (p. 3-24)	Provides the details on setting the Real-Time Workshop options when you generate code from your Simulink models to Analog Devices hardware.
Setting Real-Time Workshop Category Options (p. 3-26)	Information about setting code generation options for models
Model Reference and Link for ADI VisualDSP++ (p. 3-42)	Introduces model reference and how you use model reference with Link for Analog Devices VisualDSP++

Introducing Project Generator

Project generator provides the following features for developing projects and generating code:

- Automated project building for VisualDSP++ that lets you create VisualDSP++ projects from code generated by Real-Time Workshop and Real-Time Workshop Embedded Coder. Project generator populates projects in the VisualDSP++ development environment.
- Blocks in the library `vdspinklib` for controlling the scheduling and timing in generated code.
- Highly configurable code generation using model configuration parameters and target preferences block options.
- Capability to use Link for Analog Devices VisualDSP++ with one of two system target files to generate code specific to your processor.
- Highly configurable project build process.
- Automatic downloading and running of your generated projects on your processor.

To configure your Simulink models to use the Project Generator component, do one or both of the following tasks:

- Add a Target Preferences block from the Link for Analog Devices VisualDSP++ blockset (`vdspinklib`) to the model.
- To use the asynchronous scheduler capability in Link for ADI VisualDSP++, add one or more hardware interrupt blocks or idle task block from the Link for Analog Devices VisualDSP++ blockset (`vdspinklib`).

The following sections describe the blockset and the blocks in it, the scheduler, and the Project Generator component.

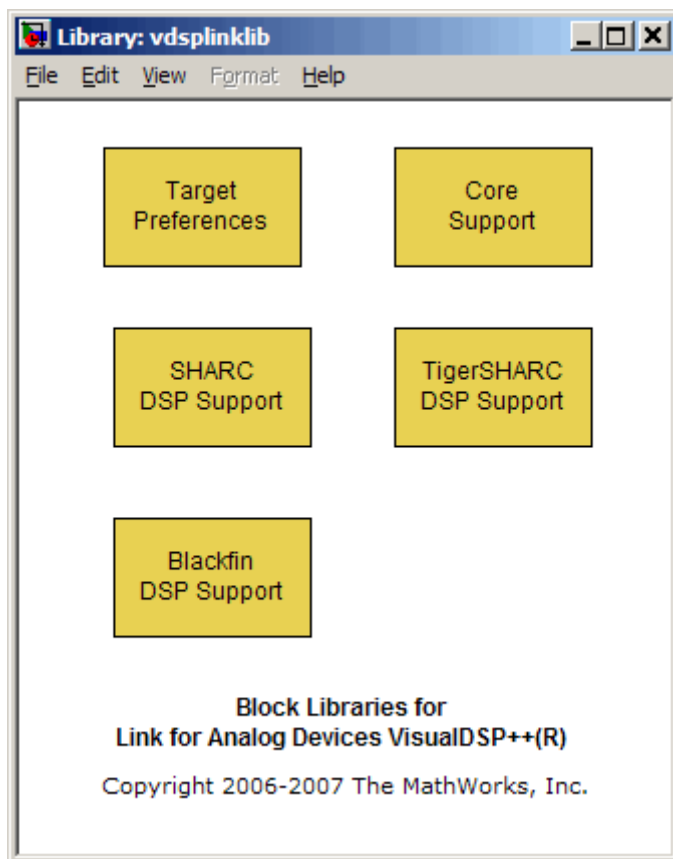
Using the Link for Analog Devices VisualDSP++ Blockset

Link for Analog Devices VisualDSP++ block library `vdspinklib` comprises block libraries that contain blocks designed for generating projects for specific processors. The following table describes these libraries.

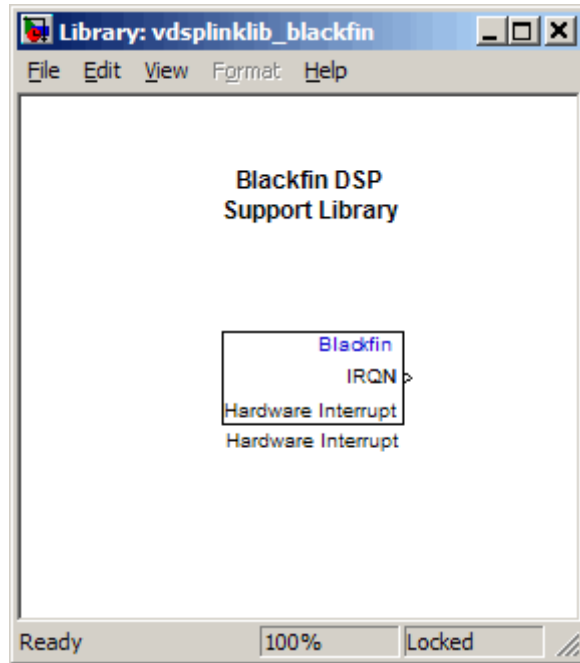
Library	Description
Blackfin DSP Support (<code>vdspinklib_blackfin</code>)	Blocks for managing memory and task scheduling on Blackfin processors
Core Support (<code>vdspinklib_coresupport</code>)	Blocks for task scheduling and manipulating memory on ADI processors
SHARC DSP Support (<code>vdspinklib_sharc</code>)	Blocks for task scheduling on SHARC processors
Target Preferences (<code>vdspinklib_tgtpref</code>)	Block that configures models for specific ADI processors
TigerSHARC DSP Support (<code>vdspinklib_tigersharc</code>)	Blocks for task scheduling on TigerSHARC processors

Blocks for the processor families are almost identical. Each block has a reference page that describes the options for the block. Use the Help browser to get more information about a block shown in any of the following figures.

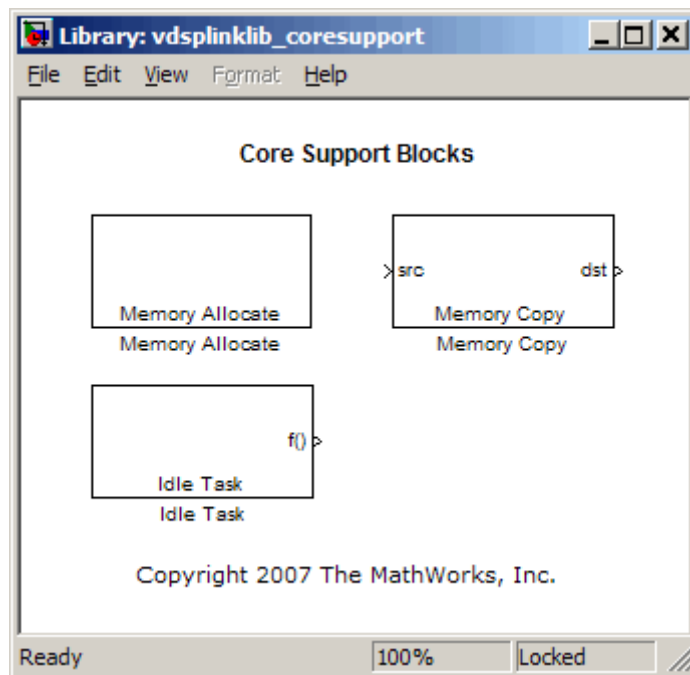
The first figure shows the main library of libraries Link for Analog Devices VisualDSP++.



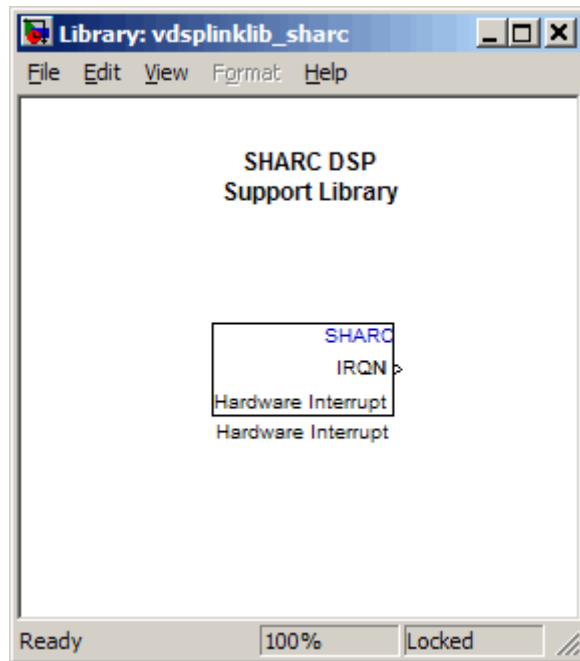
The next figure shows the Blackfin DSP Support library.



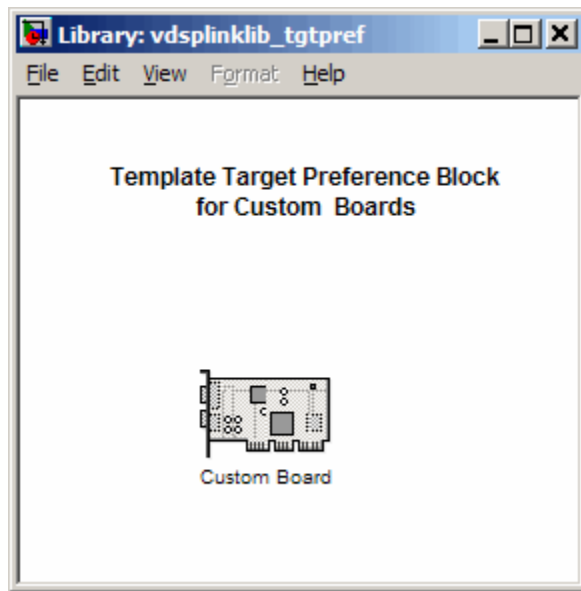
The Core Support library contains the blocks shown in the next figure.



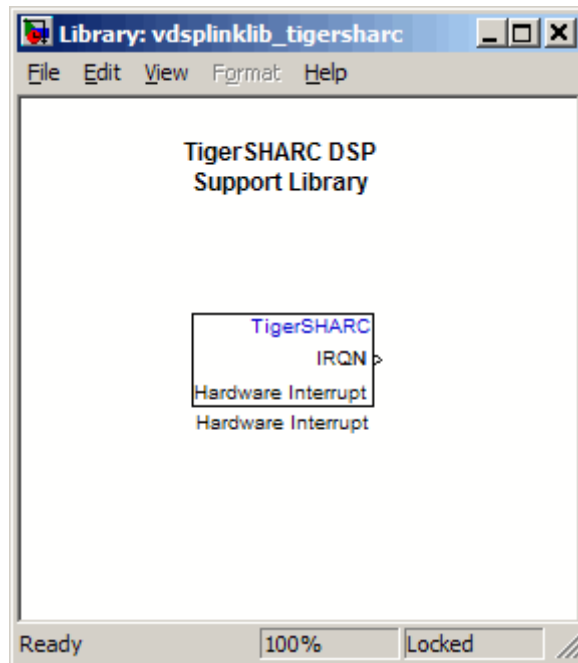
The SHARC DSP Support library contains the block in the next figure.



The target preferences library for all Analog Devices processors appears in the next figure.



The TigerSHARC DSP Support library appear in the next figure.



Schedulers and Timing

In this section...
“Timer-Based Versus Asynchronous Interrupt Processing” on page 3-10
“Synchronous Scheduling” on page 3-11
“Asynchronous Scheduling” on page 3-12
“Scheduling Blocks” on page 3-12
“Asynchronous Scheduler Examples” on page 3-12
“Uses for Asynchronous Scheduling” on page 3-15

The following sections describe how Link for Analog Devices VisualDSP++ provides timing and scheduling for generated code running on your processor.

Timer-Based Versus Asynchronous Interrupt Processing

Code generated for periodic tasks, both single- and multitasking, runs out of the context of a timer interrupt. The generated code that represents model blocks for periodic tasks runs periodically, clocked by the periodic interrupt whose period is equal to the base sample time of the model.

Note In timer-based models, the timer counts through one full base-sample-time before it creates an interrupt. When the model is finally executed, it is for time 0.

This execution scheduling scheme is not flexible enough for some systems, such as control and communication systems that must respond to asynchronous events in real time. Such systems may need to handle a variety of hardware interrupts in an asynchronous, or aperiodic, fashion.

When you plan your project or algorithm, select your scheduling technique based on your application needs.

If your application processes hardware interrupts asynchronously, add the appropriate asynchronous scheduling blocks from the Link for Analog Devices VisualDSP++ library to your model, shown in the following table.

Processor Support Library	Block Purpose	Description
Blackfin	Hardware Interrupt for asynchronous scheduling	Create interrupt service routine to handle hardware interrupt on Blackfin processors
Core DSP	Idle Task	Create task that runs as separate thread for any Analog Devices processor
SHARC	Hardware Interrupt for asynchronous scheduling	Create interrupt service routine to handle hardware interrupt on SHARC processors
Target Preferences	Target Preferences	Configure model for Analog Devices processor
TigerSHARC	Hardware Interrupt for asynchronous scheduling	Create interrupt service routine to handle hardware interrupt on TigerSHARC processors

If your application does not service asynchronous interrupts, your model should include only the algorithm and device driver blocks that specify the periodic sample times. Generating code from a model like this automatically enables and manages a timer interrupt. The periodic timer interrupt clocks the entire model.

Synchronous Scheduling

For code that runs synchronously in the context of the timer interrupt, each iteration of the model runs after an interrupt has been posted and serviced by an interrupt service routine (ISR). The code generated for Link for Analog Devices VisualDSP++ uses Timer 1. Timer 1 is configured so that the base rate sample time for the coded process corresponds to the interrupt rate. Link for Analog Devices VisualDSP++ calculates and configures the timer period to ensure the desired sample rate.

The minimum achievable base rate sample time depends on the algorithm complexity and the CPU clock speed. The maximum value depends on the maximum timer period value and the CPU clock speed.

If all the blocks in the model inherit their sample time value, and no sample time is defined explicitly, Simulink assigns a default sample time of 0.2 second.

Asynchronous Scheduling

Link for Analog Devices VisualDSP++ facilitates modeling and automatically generating code for asynchronous systems by providing interrupt and task scheduling blocks as shown in the following table:

Mode	Block
Hardware Interrupt	Blackfin, SHARC, TigerSHARC
Free-Running Task for Bare-Board Code Generation	Idle Task

Scheduling Blocks

Link for Analog Devices VisualDSP++ Hardware Interrupt blocks enable selected hardware interrupts for the Analog Devices processors, generate corresponding ISRs, and connect them to the corresponding interrupt service vector table entries.

When you connect the output of the Hardware Interrupt block to the control input of a function-call subsystem, the generated subsystem code is called from the ISRs each time the interrupt is raised.

The Idle Task block specifies one or more functions to execute as background tasks in the code generated for the model. The functions are created from the function-call subsystems to which the Idle Task block is connected.

Asynchronous Scheduler Examples

After you identify the blocks to use, you can use an asynchronous (real-time) scheduler for your application. With the asynchronous scheduler you can

define interrupts and tasks to occur when you want them to by using blocks from the following libraries:

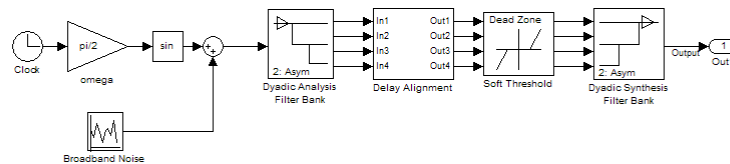
- Blackfin DSP Support
- SHARC DSP Support
- TigerSHARC DSP Support

Also, you can schedule multiple tasks for asynchronous execution using the blocks.

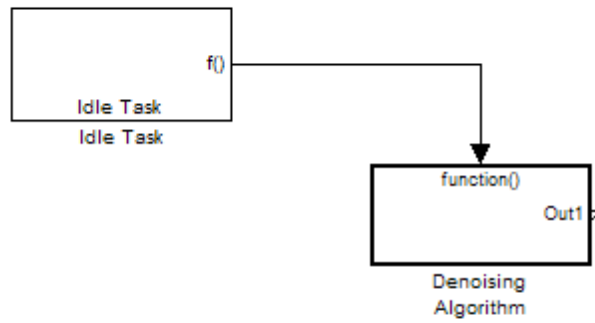
The following figures show a model updated to use the asynchronous scheduler rather than the synchronous scheduler.

Note You cannot run the example models. They provide example configurations only. They will not run or build without additional blocks.

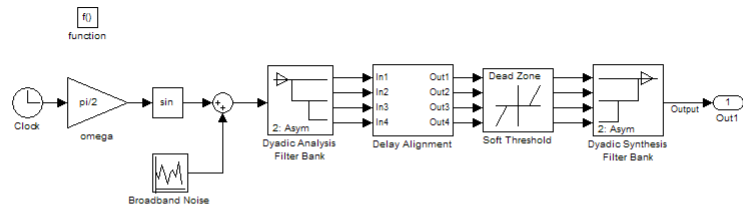
Before



After



Model Inside the Function Call Subsystem Block

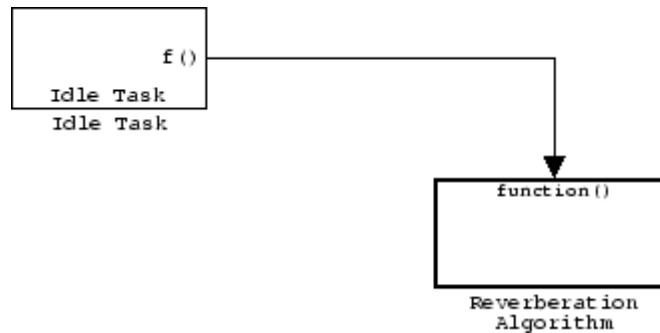


Uses for Asynchronous Scheduling

The following sections present common cases for the scheduling blocks described in the previous sections.

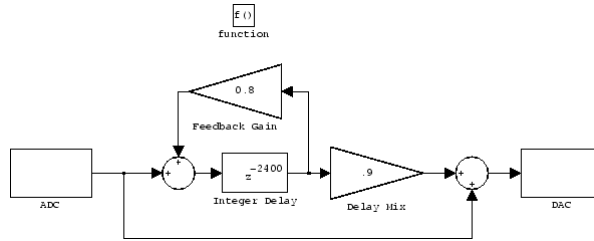
Idle Task

The following model illustrates a case where the reverberation algorithm runs in the context of a background task in bare-board code generation mode.



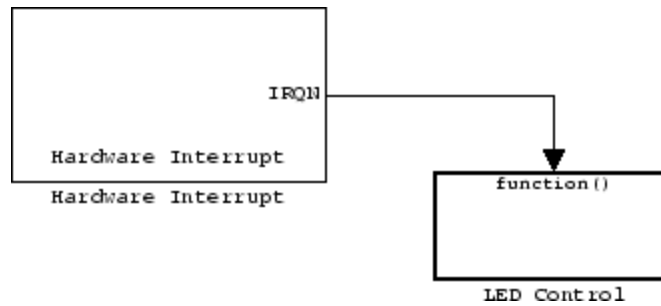
The function generated for this task normally runs in free-running mode—repetitively and indefinitely. However, the input and output blocks in this subsystem run in blocking mode. As a result, subsystem execution of the reverberation function is the same as the subsystem described for the

Free-Running Task. Task execution is data driven via a background DMA interrupt-controlled ISR, shown in the following figure.



Hardware Interrupt Triggered Task

In the next figure, you see a case where a function (control an LED) runs in the context of a hardware interrupt triggered task.



In this model, the Hardware Interrupt block installs a task that runs when it detects an external interrupt. This task then performs the specified operation.

Project Generator Tutorial

In this section...

“Building the Model” on page 3-18

“Adding the Target Preferences Block to Your Model” on page 3-18

“Specifying Simulink Configuration Parameters for Your Model” on page 3-21

In this tutorial you build a model and generate a project from the model into VisualDSP++.

Note The model demonstrates project generation only. You cannot build and run the model on your processor without additional blocks.

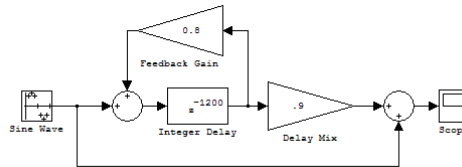
To generate a project from a model, complete the following tasks:

- 1** Use Simulink blocks, Signal Processing Blockset blocks, and blocks from other blocksets to create the model application.
- 2** Add the target preferences block from the Link for Analog Devices VisualDSP++ Target Preferences library to your model. Verify and set the block parameters for your hardware. In most cases, the default settings work fine.
- 3** Set the configuration parameters for your model, including the following parameters:
 - Solver parameters such as simulation start and solver options
 - Real-Time Workshop options such as processor configuration and processor compiler selection
- 4** Generate your project.
- 5** Review your project in VisualDSP++.

Building the Model

To build the model for audio reverberation, follow these steps:

- 1 Start Simulink.
- 2 Create a new model by selecting **File > New > Model** from the **Simulink** menu bar.
- 3 Use Simulink blocks and Signal Processing Blockset blocks to create the following model.



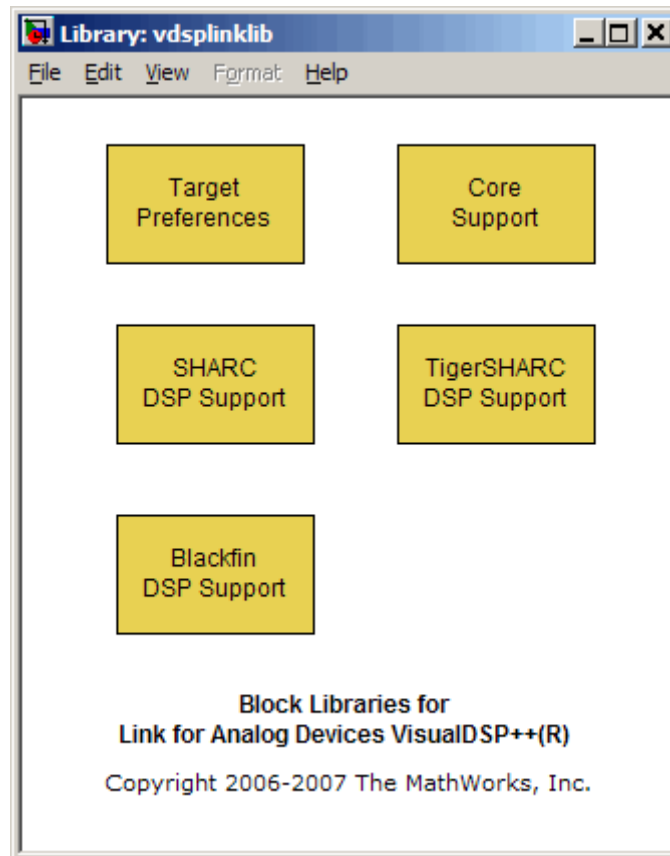
Look for the Integer Delay block in the Discrete library of Simulink and the Gain block in the Commonly Used Blocks library. Do not add the Custom Board block at this time.

- 4 Save your model with a suitable name before continuing.

Adding the Target Preferences Block to Your Model

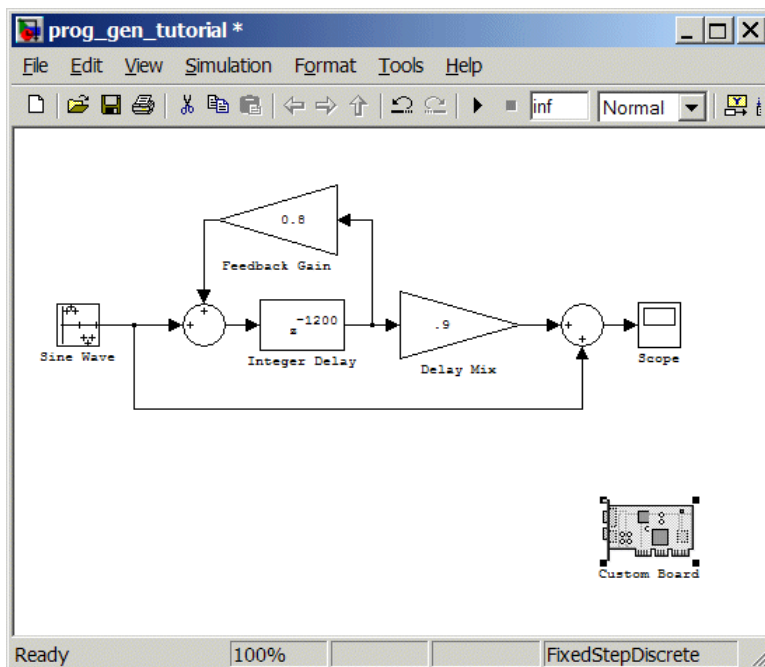
So that you can configure your model to work with Analog Devices processors, Link for Analog Devices VisualDSP++ includes a block library containing a target preferences block for Analog Devices processor, Target Preferences.

Entering `vdspinklib_tgtpref` at the MATLAB prompt opens this window showing the library blocks. This block library is included in Link for Analog Devices VisualDSP++ `vdspinklib` blockset in the Simulink Library browser.



To add the Target Preferences block to your model, follow these steps:

- 1** Double-click Link for Analog Devices VisualDSP++ in the Simulink Library browser to open the vdsplinklib blockset.
- 2** Click the library Target Preferences to see the blocks available for your processor.
- 3** Drag and drop the Custom Board block to your model as shown in the following figure.



- 4 Double-click the Custom Board block to open the block dialog box.
- 5 In the Block dialog box, select your processor from the **Processor** list.
- 6 Verify the **CPU clock** value.
- 7 Select the session name from the **Session name** list. Verify that the session processor matches the one you selected from the **Processor** list.
- 8 Review the settings on the **Memory** and **Sections** tabs to verify that they are correct for the processor you selected.
- 9 Click **OK** to close the Target Preferences dialog box.

You have completed the model. Next, configure the model configuration parameters to generate a project in VisualDSP++ from your model.

Specifying Simulink Configuration Parameters for Your Model

The following sections describe how to configure the build and run parameters for your model. Generating a project, or building and running a model on the processor, starts with configuring model options in the Configuration Parameters dialog box in Simulink.

Setting Solver Options

After you have designed and implemented your digital signal processing model in Simulink, complete the following steps to set the configuration parameters for the model:

- 1 Open the Configuration Parameters dialog box and set the appropriate options on the Solver category for your model and for Link for Analog Devices VisualDSP++.
 - Set **Start time** to 0.0 and **Stop time** to `inf` (model runs without stopping). If you set a stop time, your generated code does not honor the setting. Set this to `inf` for completeness.
 - Under **Solver options**, select the fixed-step and discrete settings from the lists.
 - Set the **Fixed step size** to Auto and the **Tasking Mode** to Single Tasking.

Note Generated code does not honor Simulink stop time from the simulation. Stop time is interpreted as `inf`. To implement a stop in generated code, you must put a Stop Simulation block in your model.

Ignore the Data Import/Export, Diagnostics, and Optimization categories in the Configuration Parameters dialog box. The default settings are correct for your new model.

Setting Real-Time Workshop Options

To configure Real-Time Workshop to use the correct processor files and to compile and run your model executable file, you set the options in the

Real-Time Workshop category of the **Select** tree in the Configuration Parameters dialog box. Follow these steps to set the Real-Time Workshop options to generate code tailored for your DSP:

- 1 Select Real-Time Workshop on the **Select** tree.
- 2 In Target selection, click **Browse** to select the system target file for Analog Devices—`vdspink_grt.tlc`. It may already be the selected target file.

Clicking **Browse** opens the **System Target File Browser** to allow you to change the system target file.

- 3 On the **System Target File Browser**, select the system target file `vdspink_grt.tlc`, and click **OK** to close the browser.

Real-Time Workshop updates the **Template makefile** and **Make command** values with the appropriate files based on your system target file selection.

Setting Link for ADI VisualDSP++ Options

After you set the Real-Time Workshop options for code generation, set the options that apply to your Analog Devices processor.

- 1 From the **Select** tree, choose Link for Analog Devices VisualDSP++ to specify code generation options that apply to the processor.
- 2 Under **Code Generation**, select the **Inline run-time library functions** option. Clear all other options.
- 3 (optional) Under **Link Automation**, provide a name for the handle in **IDE handle name**.
- 4 Set the following options in the dialog box under **Project options**:
 - Set **Project options** to Custom.
 - Set **Compiler options string** and **Linker options string** to blank.
- 5 Change the category on the **Select** tree to Hardware Implementation.


- 6 Verify that the Device type is the correct value for your processor—ADI Blackfin, ADI SHARC, or ADI TigerSHARC.
- 7 Change the category back to Link for Analog Devices VisualDSP++.
- 8 Set the following **Runtime** options:
 - **Build action:** Create_project.
 - **Interrupt overrun notification method:** Print_message.


You have configured the Real-Time Workshop options that let you generate a project for your processor. A few Real-Time Workshop categories on the **Select** tree, such as Comments, Symbols, and Optimization do not require configuration for use with Link for ADI VisualDSP++. In some cases, you may decide to set options in the other categories.

For your new model, the default values for the options in these categories are correct. For other models you develop, you may want to set the options in these categories to provide information during the build and to run TLC debugging when you generate code. Refer to your Simulink™ and Real-Time Workshop™ documentation for more information about setting the configuration parameters.

Creating Your Project

After you set the configuration parameters and configure Real-Time Workshop to create the files you need, you direct Real-Time Workshop to create your project:

- 1 Click **OK** to close the Configuration Parameters dialog box.
- 2 Click Incremental Build () on the model toolbar to generate your project into VisualDSP++.

When you press  with Create_project selected for **Build action**, the automatic build process starts VisualDSP++ and populates a new project in the development environment.

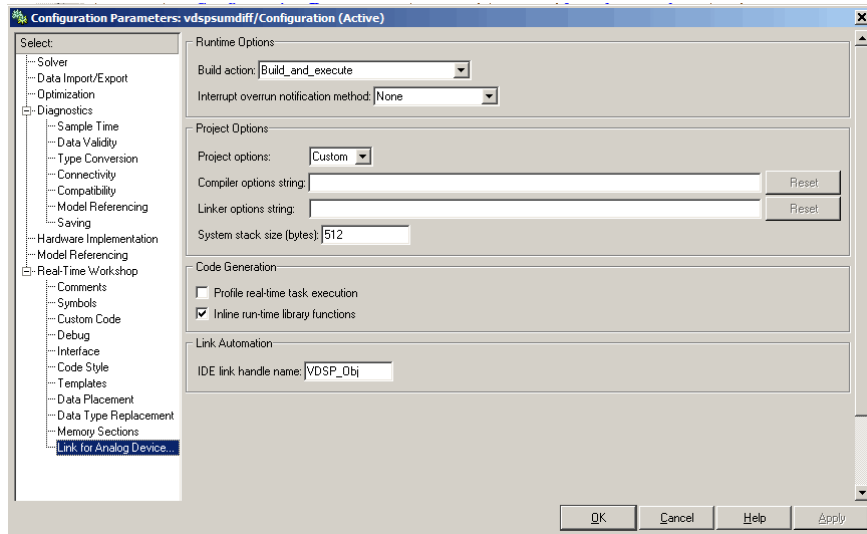
Setting Real-Time Workshop Options for Analog Devices Processors

Before you generate code with the Real-Time Workshop, set the fixed-step solver step size and specify an appropriate fixed-step solver if the model contains any continuous-time states. At this time, you should also select an appropriate sample rate for your system. Refer to the *Real-Time Workshop® User's Guide* for additional information.

Note Link for ADI VisualDSP++ does not support continuous states in Simulink models for code generation. In the **Solver options** in the Configuration Parameters dialog box, you must select **discrete** (no continuous states) as the **Type**, along with **Fixed step**.

To open the Configuration Parameters dialog box for your model, select **Simulation > Configuration Parameters** from the menu bar.

The following figure shows the Real-Time Workshop **Select** tree categories when you are using Link for Analog Devices VisualDSP++.



In the **Select** tree, the categories provide access to the options you use to control how Real-Time Workshop builds and runs your model. The first categories under Real-Time Workshop in the tree apply to all Real-Time Workshop targets including the processor and always appear on the list.

The last category under Real-Time Workshop is specific to Link for Analog Devices VisualDSP++ system target files `vdspink_grt.tlc` and `vdspink_ert.tlc` and appears when you select either target file.

When you select your target file in Target Selection on the **Real-Time Workshop** pane, the options change in the tree.

For Link for Analog Devices VisualDSP++, the target file to select is `vdspink_grt.tlc`. Selecting either the `vdspink_grt.tlc` or `vdspink_ert.tlc` adds options specific to Link for Analog Devices VisualDSP++ to the **Select** tree. The `vdspink_grt.tlc` file is appropriate for all projects. Select `vdspink_ert.tlc` when you are developing projects or code for embedded processors (requires Real-Time Workshop Embedded Coder) or you plan to use Processor-in-the-Loop features.

The following sections present each Real-Time Workshop category and the options available in each.

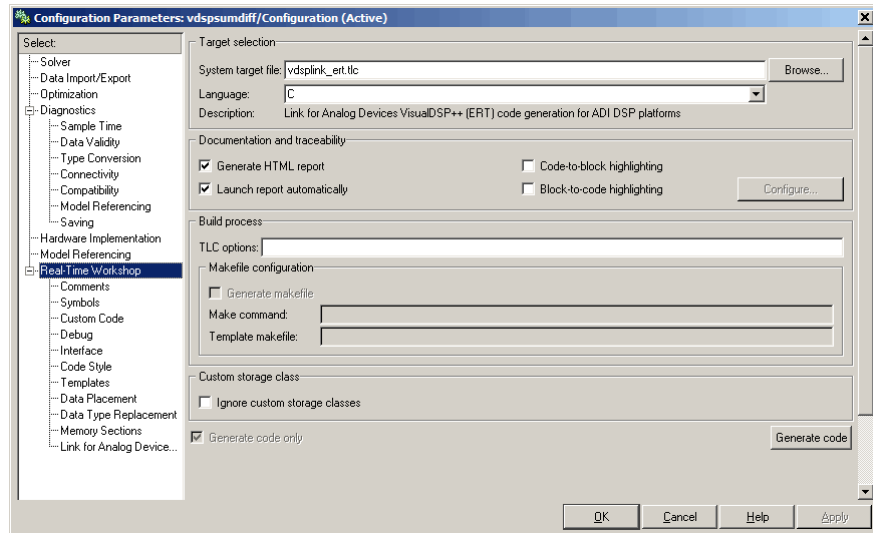
Setting Real-Time Workshop Category Options

In this section...
“Target Selection” on page 3-27
“Documentation” on page 3-27
“Build Process” on page 3-28
“Custom storage class” on page 3-29
“Debug Pane Options” on page 3-29
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“Link for Analog Devices VisualDSP++ Pane Options” on page 3-31
“Overrun Indicator and Software-Based Timer” on page 3-36
“Link for Analog Devices VisualDSP++ Default Project Options — Custom” on page 3-37
“Target Function Library and Link for ADI VisualDSP++” on page 3-38

Use the options in the **Select** tree under **Real-Time Workshop** to perform the following configuration tasks.

- Determine your processor, either Link for ADI VisualDSP++ or some other processor if you are not using Link for Analog Devices VisualDSP++.
- Specify your documentation needs.
- Configure your build process.
- Specify whether to use custom storage classes.

When you select one of the Link for Analog Devices VisualDSP++ system target files, the Link for Analog Devices VisualDSP++ category appears in the **Select** tree as shown in the following figure.



Target Selection

System target file

Clicking **Browse** opens the Target File Browser where you select `vdsplink_grt.tlc` as your Real-Time Workshop **System target file** for Link for Analog Devices VisualDSP++. When you select your target configuration, Real-Time Workshop chooses the appropriate system target file, template make file, and make command. You can also enter the target configuration filename, and Real-Time Workshop fills in the **Template makefile** and **Make command** selections.

If you are using Real-Time Workshop Embedded Coder software, select the `vdsplink_ert.tlc` target file in **System target file**.

Documentation

Two options control HTML report generation during code generation.

Generate HTML report

After you generate code, this option tells the software whether to generate an HTML report that documents the C code generated from your model. When you select this option, Real-Time Workshop writes the code generation report files in the `html` subdirectory of the build directory. The top-level HTML report file is named `modelName_codegen_rpt.html` or `subsystemname_codegen_rpt.html`. For more information about the report, refer to the online help for Real-Time Workshop. You can also use the following command at the MATLAB prompt to get more information.

```
docsearch 'Generate HTML report'
```

Launch report automatically

This option direct Real-Time Workshop to open a MATLAB Web browser window and display the code generation report. When you clear this option, you can open the code generation report (`modelName_codegen_rpt.html` or `subsystemname_codegen_rpt.html`) manually in a MATLAB Web browser window or in another Web browser manually.

Build Process

Template makefile

Real-Time Workshop uses template makefiles to generate the makefile for building the executable file. During the automatic build process, MATLAB issues the `make_rtw` command. `make_rtw` extracts information from the template makefile `vdspLink_grt.tmf` and creates the actual makefile `vdspLink.mk`. When Real-Time Workshop compiles the model, it uses the actual makefile to select the compiler to use to generate the compiled code.

Make command

When you generate code from your digital signal processing application, select **Generate makefile** and use the standard command `make_rtw` as the **Make command**. In the **Build process** area in the Real-Time Workshop category, enter `make_rtw` for the **Make command**. Parameters you set in this dialog box belong to the model you are building. They are saved with the model and stored in the model file.

Custom storage class

When you generate code from a model employing custom storage classes (CSC), clear **Ignore custom storage classes**. This setting is the default value for Link for Analog Devices VisualDSP++ and for Real-Time Workshop Embedded Coder.

When you select **Ignore custom storage classes**, storage class attributes and signals are affected in the following ways:

- Objects with CSCs are treated as if you set their storage class attribute to Auto.
- The storage class of signals that have CSCs does not appear on the signal line, even when you select Storage class from **Format > Port/Signals Display** in your Simulink menus.

Ignore custom storage classes lets you switch to a processor that does not support CSCs, such as the generic real-time target (GRT), without reconfiguring your parameter and signal objects.

Generate code only

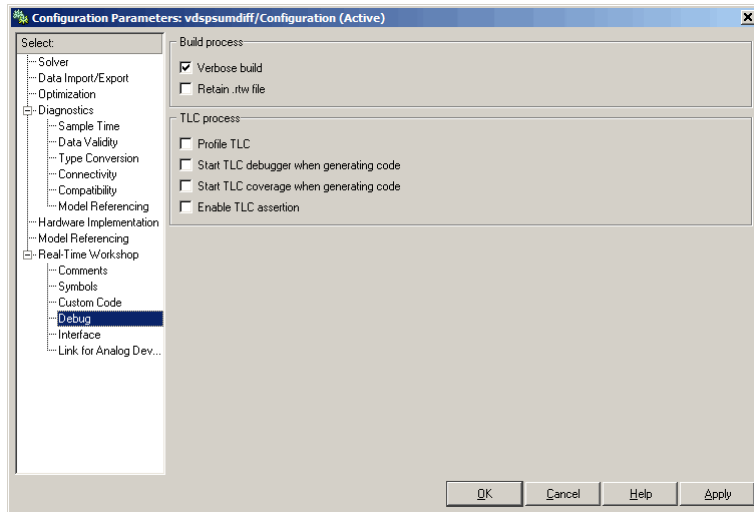
The **Generate code only** option does not apply to targeting with Link for Analog Devices VisualDSP++. To generate source code without building and executing the code on your processor, select Link for Analog Devices VisualDSP++ from the **Select** tree. Then, under **Runtime**, select `Create_project` for **Build action**.

Debug Pane Options

Real-Time Workshop uses the Target Language Compiler (TLC) to generate C code from the `model.rtw` file. The TLC debugger helps you identify programming errors in your TLC code. Using the debugger, you can perform the following actions:

- View the TLC call stack.
- Execute TLC code line-by-line.
- Analyze or change variables in a specified block scope.

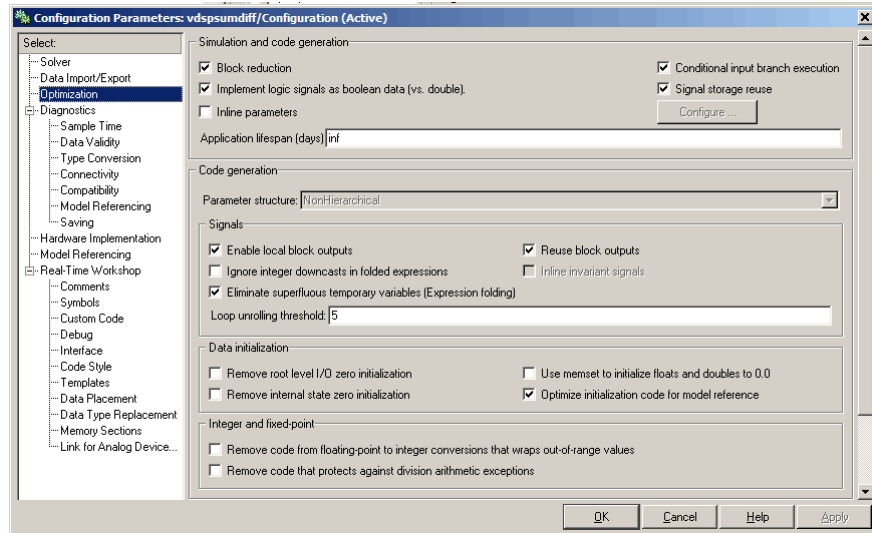
When you select Debug from the **Select** tree, you see the Debug options as shown in the next figure. In this dialog box, you set options that are specific to Real-Time Workshop process and TLC debugging.



For details about using the options in Debug, refer to “About the TLC Debugger” in your Real-Time Workshop Target Language Compiler documentation.

Optimization Pane Options

On the Optimization pane in the Configuration Parameters dialog box, you set options for the code that Real-Time Workshop generates during the build process. Use these options to tailor the generated code to your needs. Select Optimization from the **Select** tree on the Configuration Parameters dialog box. The figure shows the Optimization pane when you select the system target file vdsplink_grt.tlc under **Real-Time Workshop system target file**.



These options are typically selected for Real-Time Workshop to provide optimized code generation for common code operations:

- **Conditional input branch execution**
- **Signal storage reuse**
- **Enable local block outputs**
- **Reuse block outputs**
- **Eliminate superfluous temporary variables (Expression folding)**
- **Loop unrolling threshold**
- **Optimize initialization code for model reference**

For more information about using these and the other Optimization options, refer to the Real-Time Workshop documentation.

Link for Analog Devices VisualDSP++ Pane Options

On the select tree, the Link for Analog Devices VisualDSP++ category provides options in these areas:

- **Link Automation** — Export a handle to your MATLAB workspace.
- **Code Generation** — Configure your code generation requirements, such as enabling real-time task execution profiling.
- **Project Options** — Set build options for your project code generation, including compiler and linker settings.
- **Runtime** — Set options for run-time operations, like the build action.
- **Processor-in-the-loop (PIL) verification** — Enable processor in the loop capability for your project.

Link Automation

When you use Real-Time Workshop to build a model to an Analog Devices processor, Link for ADI VisualDSP++ makes a connection between MATLAB and VisualDSP++. MATLAB represents that connection as an `adivdsp` object. The properties of the `adivdsp` object contain information about the IDDE instance it refers to, such as the session and processor it accesses. In this pane, the **IDE link handle name** option instructs Link for Analog Devices VisualDSP++ to export the `adivdsp` object created during code generation to your MATLAB workspace with the name you enter. Replace the default value `VDSP_obj` with your own name for the object to export.

Code Generation

From this category, you select options that define the way your code is generated:

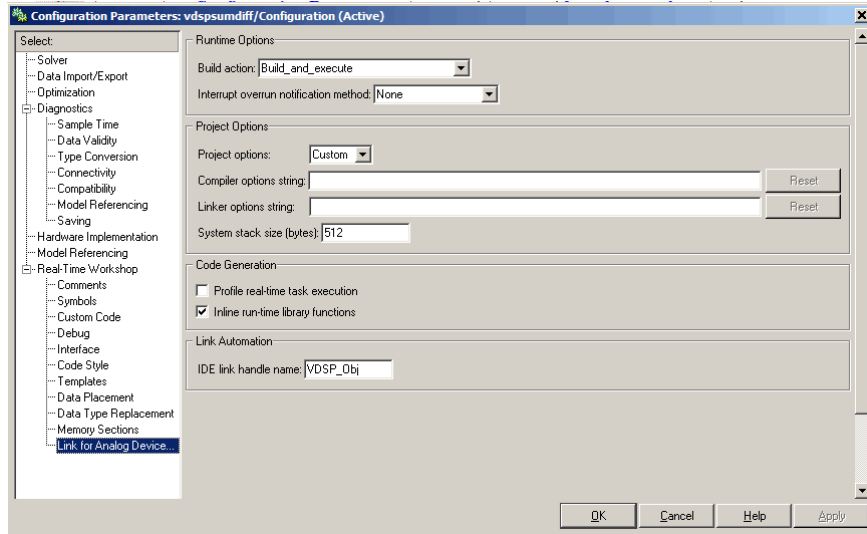
- **Profile real-time task execution**
- **Inline run-time library functions**

To enable the real-time execution profile capability, select **Profile real-time task execution**. When you select this option, the build process instruments your code to provide performance profiling at the task level. When you run your code, the executed code reports the profiling information in both a graphical presentation and an HTML report form.

To allow you to specify whether the functions generated from blocks in your model are used inline or by pointers, **Inline run-time library functions** tells the compiler to inline each Signal Processing blockset and Video and

Imaging blockset function. Using inline functions optimizes your code to run more efficiently. However, such optimization requires more memory.

As shown in the following figure, the default setting uses inlining to optimize your generated code.



When you designate a block function as inline, the compiler replaces each call to a block function with the equivalent function code from the static run-time library. If your model use the same block four times, your generated code contains four copies of the function.

While this redundancy uses more memory, inline functions run more quickly than calls to the functions outside the generated code.

Project Options

Before you run your model as an executable on any processor, configure the Project options for the model. By default, the setting for the project options is Custom, which applies MathWorks specified compiler and linker settings for your generated code.

Compiler options string

To let you determine the degree of optimization provided by the Analog Devices optimizing compiler, you enter the optimization level to apply to files in your project. For details about the compiler options, refer to your VisualDSP++ documentation. When you create new projects, Link for Analog Devices VisualDSP++ sets the optimization to `Function(-o2)`.

Linker options string

To let you specify the options provided by the Analog Devices linker during link time, you enter the linker options as a string. For details about the linker options, refer to your VisualDSP++ documentation. When you create new projects, Link for Analog Devices VisualDSP++ sets no linker options.

System stack size (bytes)

Enter the amount of memory to use for the stack. For more information on memory requirements, refer to Local block outputs on the **Optimization** pane of the Configuration Parameters dialog box. The block output buffers are placed on the stack until the stack memory is fully allocated. When the stack memory is full, the output buffers go in global memory. Refer to the online Help system for more information about Real-Time Workshop options for configuring and building models and generating code.

Runtime

Before you run your model as an executable on any Analog Devices processor, you must configure the run-time options for the model.

By selecting values for the options available, you configure the operation of your model build process and overrun handling.

Build action

To specify to Real-Time Workshop what to do when you click **Build**, select one of the following options.:

- `Create_project` — Directs Real-Time Workshop to start VisualDSP++ and populate a new project with the files from the build process. This option offers a convenient way to build projects in VisualDSP++.

- `Archive_library` — Directs Real-Time Workshop to archive the project for this model. Use this option when you plan to use the model in a model reference application. Model reference requires that you archive your VisualDSP++ projects for models that you use in model referencing.
- `Build` — Builds the executable file, but does not download the file to your processor.
- `Build_and_execute` — Directs Real-Time Workshop to build, download, and run your generated code as an executable on your processor.
- `Create_processor_in_the_loop_project` — Directs the Real-Time Workshop code generation process to create PIL algorithm object code as part of the project build.

Your selection for **Build action** determines what happens when you click **Build** or press **Ctrl+B**. Your selection tells Real-Time Workshop when to stop the code generation and build process.

To run your model on the processor, select the default build action, `Build_and_execute`. Real-Time Workshop then automatically downloads and runs the model on your processor.

Note When you build and execute a model on your processor, the Real-Time Workshop build process resets the processor automatically. You do not need to reset the board before building models.

Interrupt overrun notification method

To enable the overrun indicator, choose one of three ways for the processor to respond to an overrun condition in your model:

- `None` — Ignore overruns encountered while running the model.
- `Print_message` — When the processor encounters an overrun condition, it prints a message to the standard output device, `stdout`.
- `Call_custom_function` — Respond to overrun conditions by calling the custom function you identify in **Interrupt overrun notification function**.

Interrupt overrun notification function

When you select `Call_custom_function` from the **Interrupt overrun notification method** list, you enable this option. Enter the name of the function the processor should use to notify you that an overrun condition occurred. The function must exist in your code on the processor.

Overrun Indicator and Software-Based Timer

Link for Analog Devices VisualDSP++ includes software that generates interrupts in models that use multiple clock rates. In the following cases, the overrun indicator does not work:

- In multirate systems where the rate in the model is not the same as the base clock rate for your model. In such cases, the timer in Link for Analog Devices VisualDSP++ provides the interrupts for setting the model rate.
- In models that do not include ADC or DAC blocks. In such cases, the timer provides the software interrupts that drive model processing.

PIL block action

If you have Real-Time Workshop Embedded Coder installed and you select the `vdspink_ert.tlc` system target file, you can choose to use the processor-in-the-loop (PIL) feature provided by Link for Analog Devices VisualDSP++. Selecting `Create_processor_in_the_loop_project` for the **Build action** enables the **PIL block action** option. **PIL block action** specifies whether Real-Time Workshop builds the PIL block and downloads the block to the processor.

Choose one of the following three actions for creating a PIL block:

- **None** — Configures model to generate a VisualDSP++ project that contains the PIL algorithm code. Does not build the PIL object code or block. The new project will not compile in VisualDSP++.
- **Create PIL block** — Creates a PIL block, places the block in a new model, and then stops without building or downloading the block. The resulting project will not compile in VisualDSP++.
- **Create PIL block_build_and_download** — Builds and downloads the PIL application to the processor after creating the PIL block. Adds PIL

interface code that exchanges data with Simulink. Use this selection to update the algorithmic code in an existing PIL block in a model.

Your selections affect how you use the resulting PIL block. The following list describes the build process and actions you take based on the **PIL block action** setting:

- When you click **Build** on the PIL dialog box, the build process adds the PIL interface code to the project and compiles the project in VisualDSP++.
- If you select Create PIL block, you can build manually from the right-click context menu on the PIL block.
- After you select Create PIL Block, copy the PIL block into your model to replace the original subsystem. Save the original subsystem in a different model so you can restore in the future. Click **Build** to build your model with the PIL block in place.
- Add the PIL block to your model to use cosimulation to compare PIL results with the original subsystem results. Refer to the demo “Code Generation Workflow”
in the product demos Link for Analog Devices VisualDSP++
- To use the PIL block in a project after you selected None or Create PIL block for **Block action** when you built the project, click **Build** followed by **Download** in the PIL block dialog box.

Link for Analog Devices VisualDSP++ Default Project Options – Custom

Although VisualDSP++ offers standard project configurations, Release and Debug, models you build with Link for Analog Devices VisualDSP++ use Custom for a custom configuration that provides a third combination of build and optimization.

Project configurations define sets of project build options. When you specify the build options at the project level, the options apply to all files in your project. For more information about the build options, refer to your Analog Devices VisualDSP++ documentation.

The default settings for Custom are the same as the Release project configuration in VisualDSP++, except for the compiler options discussed in

the next section “Default Project Options in Custom” on page 3-38. Custom uses different compiler optimization levels to preserve important features of the generated code.

Default Project Options in Custom

When you create a new project or build a model to your Analog Devices processor, your project and model inherit the build configuration settings from the configuration Custom. The settings in Custom differ from the settings in the default Debug and Release configurations in VisualDSP++ in the compiler settings.

For the compiler options, Custom uses the Function(-o2) compiler setting. The VisualDSP++ default Release configuration uses File(-o3), a slightly more aggressive optimization model.

For memory configuration, where Release uses the default memory model that specifies near functions and data, Custom specifies near functions and data—the -m11 memory model—because some custom hardware might not support far data or aggregate data. Your VisualDSP++ documentation provides complete details on the compiler build options.

You can change the individual settings or the build configuration within VisualDSP++. Build configuration options that do not appear on these panes default to match the settings for the Release build configuration in VisualDSP++.

Target Function Library and Link for ADI VisualDSP++

If you are using `vdspink_ert.tlc` as your system target file, Link for ADI VisualDSP++ software supports generating code that is optimized for the processor by using compiler intrinsics and assembly code to replace certain mathematical operator functions. Link for ADI VisualDSP++ accomplishes this optimization through the Target Function Library (TFL) replacement mechanism that Real-Time Workshop Embedded Coder provides. TFL replacement requires Real-Time Workshop Embedded Coder and the embedded real-time target—`vdspink_ert.tlc`.

Some code generation stages launch TFL queries. Based on the processor you select, TFL replaces the default Real-Time Workshop sum and

multiply functions and other arithmetic and mathematical operators with processor-specific compiler intrinsics and assembly code functions. For more general information about TFL, look for TFL in the Interface options in “Configuring Real-Time Workshop Code Generation Parameters”.

TFL Replacement Functions

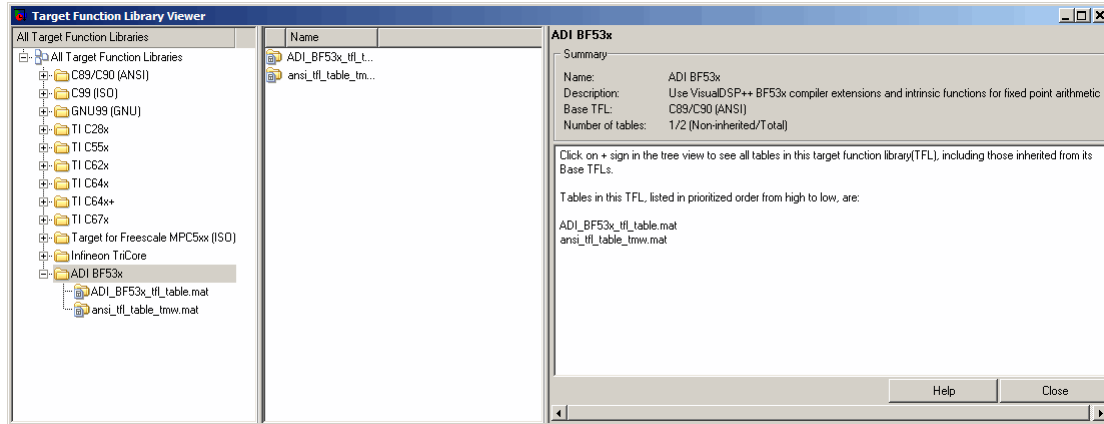
When you enable TFL replacement, Real-Time Workshop uses compiler intrinsics and assembly code functions provided by Link for ADI VisualDSP++ to replace the sums and multiplies in your generated code. The replacement functions provide optimized operations that enable your generated code to run more efficiently and quickly.

TFL Viewer

TFL replacement does not provide direct feedback when you generate code. To help you review the TFL replacement operators and code, Real-Time Workshop Embedded Coder provides the TFL Viewer. To start the viewer with all of the available math libraries listed, enter the following command at the MATLAB prompt:

```
RTW.viewTFL
```

The viewer enables you to see the content of target function library tables that were created using Real-Time Workshop Embedded Coder. The following figure shows the TFL viewer displaying the libraries for the Blackfin 53x processor family. Follow the instructions in the viewer to see the operators and the TFL code associated with each operator.



Enabling TFL for Code Generation

You use an option in the Configuration Parameters for your model to enable TFL replacement during code generation. Perform the following steps to enable the TFL replacement process when you generate code from a model.

To use the TFL replacement capability when you generate code, you must install Real-Time Workshop Embedded Coder and select the system target file `vdsplink_ert.tlc`.

- 1 Open the Configuration Parameters for your model by selecting **Simulation > Configuration Parameters** from the model menu bar.
- 2 On the **Select** tree in the Configuration Parameters dialog box, choose Real-Time Workshop.
- 3 Set the **System target file** to `vdsplink_ert.tlc`. Use **Browse** to select the file.
- 4 On the **Select** tree, choose Interface.
- 5 From the **Target function library** list, select the Analog Devices processor family that matches your processor.
- 6 Click **OK** to save your changes and close the dialog box.

With TFL enabled, your generated code uses the TFL replacement libraries provided for your processor.

Model Reference and Link for ADI VisualDSP++

In this section...

“How Model Reference Works” on page 3-42

“Using Model Reference with Link for ADI VisualDSP++” on page 3-43

“Configuring Targets to Use Model Reference” on page 3-45

Model reference lets your model include other models as modular components. This technique is useful because it provides the following capabilities:

- Simplifies working with large models by letting you build large models from smaller ones, or even large ones.
- Lets you generate code once for all the modules in the entire model and then only regenerate code for modules that change.
- Lets you develop the modules independently.
- Lets you reuse modules and models by reference, rather than including the model or module multiple times in your model. Also, multiple models can refer to the same model or module.

Your Real-Time Workshop documentation provides much more information about model reference.

How Model Reference Works

Model reference behaves differently in simulation and in code generation. For this discussion, you need to know the following terms:

- The *Top model* is the root model block or model. It refers to other blocks or models. In the model hierarchy, this is the topmost model.
- *Referenced models* are blocks or models that other models reference, such as models the top model refers to. All models or blocks below the top model in the hierarchy are reference models.

The following sections describe briefly how model reference works. More details are available in your Real-Time Workshop documentation in the online Help system.

Model Reference in Simulation

When you simulate the top model, Real-Time Workshop detects that your model contains referenced models. Simulink generates code for the referenced models and uses the generated code to build shared library files for updating the model diagram and simulation. It also creates an executable (.mex file) for each reference model that is used to simulate the top model.

When you rebuild reference models for simulations or when you run or update a simulation, Simulink rebuilds the model reference files. Whether reference files or models are rebuilt depends on whether and how you change the models and on the **Rebuild options** settings. You can access these setting through the **Model Reference** pane of the Configuration Parameters dialog box.

Model Reference in Code Generation

Real-Time Workshop requires executables to generate code from models. If you have not simulated your model at least once, Real-Time Workshop creates a .mex file for simulation.

Next, for each referenced model, the code generation process calls `make_rtw` and builds each referenced model. This build process creates a library file for each of the referenced models in your model.

After building all the referenced models, Real-Time Workshop calls `make_rtw` on the top model, linking to all the library files it created for the associated referenced models.

Using Model Reference with Link for ADI VisualDSP++

With few limitations or restrictions, Link for Analog Devices VisualDSP++ provides full support for generating code from models that use model reference.

Build Action Setting

The most important requirement for using model reference with the Analog Devices targets is that you must set the **Build action** (select **Configuration Parameters > Link for Analog Devices VisualDSP++**) for all models referred to in the simulation to `Archive_library`.

To set the build action, perform the following steps:

- 1 Open your model.
- 2 Select **Simulation > Configuration Parameters** from the model menus.
The Configuration Parameters dialog box opens.
- 3 From the **Select** tree, choose Link for Analog Devices VisualDSP++.
- 4 In the right pane, under **Runtime**, select set Archive_library from the **Build action** list.

If your top model uses a reference model that does not have the build action set to Archive_library, the build process automatically changes the build action to Archive_library and issues a warning about the change.

Selecting the Archive_library setting removes the following options from the dialog box:

- **Interrupt overrun notification method**
- **Compiler options string**
- **Linker options string**
- **System stack size (bytes)**
- **Profile real-time task execution**

Target Preferences Blocks in Reference Models

Each referenced model and the top model must include a Target Preferences block for the correct processor. You must configure all the Target Preferences blocks for the same processor.

The referenced models need target preferences blocks to provide information about which compiler and which archiver to use. Without these blocks, the compile and archive processes do not work.

By design, model reference does not allow information to pass from the top model to the referenced models. Referenced models must contain all the

necessary information, which the Target Preferences block in the model provides.

Other Block Limitations

Model reference with Link for Analog Devices VisualDSP++ does not allow you to use the following blocks or S-functions in reference models:

- No blocks from the Link for Analog Devices VisualDSP++[®]Library (vdspLinkLib) (because these are noninlined S-functions)
- No noninlined S-functions

Configuring Targets to Use Model Reference

When you create models to use in Model Referencing, keep in mind the following considerations:

- Your model must use a system target file derived from the ERT or GRT targets files.
- When you generate code from a model that references other models, you must configure the top-level model and the referenced models for the same system target file.
- Real-Time Workshop builds and Link for ADI VisualDSP++ do not support external mode in model reference. If you select the external mode option, it is ignored during code generation.
- Your TMF must support use of the shared utilities directory, as described in Supporting Shared Utility Directories in the Build Process in the Real-Time Workshop documentation.

To use an existing processor, or a new processor, with Model Reference, set the `ModelReferenceCompliant` flag for the processor. For information about setting this option, refer to `ModelReferenceCompliant` in the online Help system.

If you start with a model that was created prior to MATLAB release R14SP3, use the following command to set the `ModelReferenceCompliant` flag to On to make your model compatible with model reference:

```
set_param(bdroot, 'ModelReferenceCompliant', 'on')
```

Code that you generate from Simulink models by using Link for ADI VisualDSP++ automatically include the model reference capability. You do not need to set the flag.

Verification

What is Verification? (p. 4-2)	Explains verification and what it covers
Using Processor-in-the-Loop (p. 4-3)	Introduces PIL in Link for ADI VisualDSP++
Real-Time Execution Profiling (p. 4-9)	Discusses execution profiling

What is Verification?

Verification consists broadly of running generated code on a processor and verifying that the code does what you intend. The components of Link for ADI VisualDSP++ combine to provide tools that help you verify your code during development by letting you run portions of simulations on your hardware and profiling the executing code.

Using the Automation Interface and Project Generator components, Link for ADI VisualDSP++ offers the following verification functions:

- Processor-in-the-Loop — A technique to help you evaluate how your process runs on your processor
- Real-Time Task Execution Profiling — A tool that lets you see how the tasks in your process run in real-time on your processor hardware

Using Processor-in-the-Loop

In this section...
“Processor-in-the-Loop Overview” on page 4-3
“PIL Block” on page 4-6
“Creating and Using PIL Blocks” on page 4-6

Processor-in-the-loop provides one verification capability in your development process.

Processor-in-the-Loop Overview

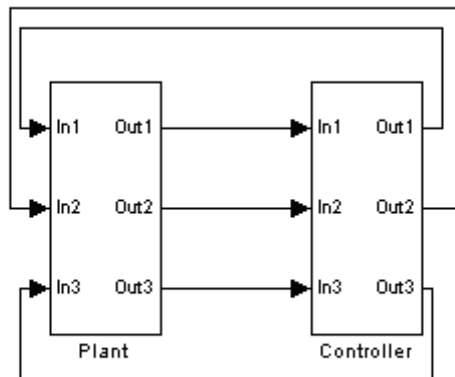
Processor-in-the-loop (PIL) cosimulation is a technique designed to help you evaluate how well a candidate algorithm, such as a control system, operates on the actual processor selected for the application.

The term *cosimulation* reflects a division of labor in which Simulink models the plant, while code generated from the controller subsystem runs on the actual processor hardware.

During the Real-Time Workshop Embedded Coder code generation process, you can create a PIL block from one of several Simulink components including a model, a subsystem in a model, or subsystem in a library. You then place the generated PIL block inside a Simulink model that serves as the test harness and run tests to evaluate the processor-specific code execution behavior.

Why Use Cosimulation?

PIL cosimulation is particularly useful for simulating, testing, and validating a controller algorithm in a system comprising a plant and a controller. In a classic closed-loop simulation, Simulink and Stateflow® model such a system as two subsystems with the signals transmitted between them, as shown in the following block diagram:



Your starting point in developing a plant/controller system is to model the system as two subsystems in closed-loop simulation. As your design progresses, you can use Simulink external mode with standard Real-Time Workshop targets (such as GRT or ERT) to help you model the control system separately from the plant.

However, these simulation techniques do not help you account for restrictions and requirements imposed by the hardware, such as limited memory resources, or behavior of processor-specific optimized code. When you finally reach the stage of deploying controller code on the processor hardware, you may need to make extensive adjustments to the controller system. After you make these adjustments, your deployed system may diverge significantly from the original model. Such discrepancies can create difficulties if you need to return to the original model and change it.

PIL cosimulation addresses these issues by providing an intermediate stage between simulation and deployment. In a PIL cosimulation, the processor participates fully in the simulation loop—hence the term *processor-in-the-loop*.

Definitions

PIL Algorithm

The algorithmic code, such as the control algorithm, to be tested during the PIL cosimulation. The PIL algorithm resides in compiled object form to allow verification at the object level.

PIL Application

The executable application to run on the processor. The PIL application is created by linking the PIL algorithm object code with some wrapper code (or test harness) that provides an execution framework that interfaces to the PIL algorithm.

The wrapper code includes the `string.h` header file so that the `memcpy` function is available to the PIL application. The PIL application uses `memcpy` to facilitate data exchange between Simulink and the cosimulation processor.

Note Whether the PIL algorithm code under test uses `string.h` is independent of the use of `string.h` by the wrapper code, and depends on the implementation of the algorithm in the generated code.

How Cosimulation Works

In a PIL cosimulation, Real-Time Workshop generates an executable application for the PIL algorithm. This code runs (in simulated time) on a processor platform. The plant model remains in Simulink without the use of code generation.

During PIL cosimulation, Simulink simulates the plant model for one sample interval and exports the output signals (`outn` of the plant) to the processor platform via VisualDSP++. When the processor platform receives signals from the plant model, it executes the PIL algorithm for one sample step. The PIL algorithm returns its output signals (`ontn` of the algorithm) computed during this step to Simulink in `inn`, via the VisualDSP++ interface. At this point, one sample cycle of the simulation is complete and the plant model proceeds to the next sample interval. The process repeats and the simulation progresses.

PIL tests do not run in real time. After each sample period, the simulation halts to ensure that all data has been exchanged between the Simulink test

harness and object code. You can then check functional differences between the model and generated code.

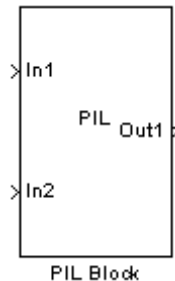
PIL Block

The PIL cosimulation block is the Simulink block interface to PIL and the interface between the Simulink plant model and the executable application running on the processor. The Simulink inputs and outputs of the PIL cosimulation block are configured to match the input and output specification of the PIL algorithm.

The block is a basic building block that enables you to perform these operations:

- Select a PIL algorithm
- Build and download a PIL application
- Run a PIL cosimulation

The PIL block inherits the shape and signal names from the parent subsystem, like those in the following example. This inheritance feature is convenient for copying the PIL block into the model to replace the original subsystem for cosimulation.



Creating and Using PIL Blocks

Using PIL and PIL blocks to verify your processes begins with a Simulink model of your process. To see an example of one such model used to implement PIL, refer to the demo Comparing Simulation and Processor Implementation

with Processor-in-the Loop (PIL) (`pilsumdiffdemo.mdl`) in the demos for Link for ADI VisualDSP++.

Note While your models can have multiple PIL blocks for different subsystems, you cannot have more than one PIL block for the same subsystem. Including multiple PIL blocks for the same subsystem causes errors and incorrect results because the PIL blocks try to run the same code.

To create and use a PIL block, perform the following tasks:

1 Develop the model of the process to simulate.

Use Simulink to build a model of the process to simulate. The blocks in the library `vdspinklib` can help you set up the timing and scheduling for your model.

For information about building Simulink models, refer to *Getting Started with Simulink* in the online Help system.

2 Convert your process to a masked subsystem in your model.

For information about how to convert your process to a subsystem, refer to *Creating Subsystems* in *Using Simulink* or in the online Help system.

3 Open the new masked subsystem and add a target preferences block to the subsystem.

The block library `vdspinklib` contains the Target Preferences block to add to your system. Configure the Target Preferences block for your processor. For details about the options on the Target Preferences block, refer to the Target Preferences block reference in the online Help system.

4 Configure your model to enable it to generate PIL algorithm code and a PIL block from your subsystem.

- From the model menu bar, go to **Simulation > Configuration Parameters** in your model to open the Configuration Parameters dialog box.

- b** Choose **Real-Time Workshop** from the **Select** tree. Set the configuration parameters for your model as required by Link for ADI VisualDSP++. Get more information about setting the Real-Time Workshop parameters in “Setting Real-Time Workshop Options for Analog Devices Processors” on page 3-24 in the online Help system.
 - c** Under **Target selection**, set the **System target file** to `vdsplink_ert.tlc` (PIL requires Real-Time Workshop Embedded Coder).
- 5** Configure the model to perform PIL building and PIL block creation.
- a** Select **Link for ADI VisualDSP++** on the **Select** tree.
 - b** Under **Build action**, select **Create_processor_in_the_loop_project** from the list to enable PIL block and PIL project generation.
 - c** Click **OK** to close the Configuration Parameters dialog box.
- 6** To create the PIL block, right-click the masked subsystem in your model and select **Real-Time Workshop > Build Subsystem** from the context menu.

This step builds the PIL algorithm object code and a PIL block that corresponds to the subsystem, with the same inputs and outputs. Follow the progress of the build process in the MATLAB command window.

A new model window opens and the new PIL block appears in it.

- 7** Copy the new PIL block from the new model to your model, either in parallel to your masked subsystem to cosimulate the processes, or replace your subsystem with the PIL block.

To see the PIL block used in parallel to a masked subsystem, refer to the demo Comparing Simulation and Processor Implementation with Processor-in-the Loop (PIL) (`pilsumdiffdemo.mdl`) in the demos for Link for ADI VisualDSP++.

- 8** Click **Simulation > Start** to run the PIL simulation and view the results.

Real-Time Execution Profiling

In this section...
“Overview” on page 4-9
“Profiling Program Execution” on page 4-9

Overview

The real-time execution profile capability in Link for ADI VisualDSP++ uses a set of utilities that record, upload, and analyze the execution profile data for synchronous and asynchronous tasks in your generated code.

The profiler generates output in the following formats:

- Graphical display that shows task activation, preemption, task resumption, and task completion. All of the data is presented in the form of a MATLAB graphic with the data presented by model rates and execution time.
- An HTML report that provides statistical data about the execution of each task in the running process.


In combination, the reports provide a detailed analysis of how your code runs on the processor.

Profiling Program Execution

To configure a model to use execution profiling, perform the following steps:

- 1 Open the Configuration Parameters dialog for your model.
- 2 Select `Link for ADI VisualDSP++` from the **Select** tree.
- 3 Select **Profile real-time task execution** to enable real-time task profiling.
- 4 Assign a name for the object handle in **IDE link handle name**. Link for ADI VisualDSP++ exports this object to your MATLAB workspace with the name you enter.
- 5 Click **OK** to close the Configuration Parameters dialog box.

To run your simulation and then view the execution profile for your model:

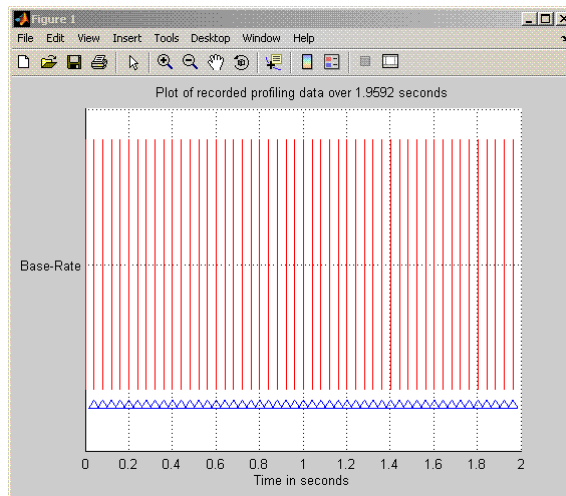
- 1 Click **Incremental build** () on the model toolbar to generate, build, load, and run your code on the processor.
- 2 Switch to the IDDE and halt the running program in VisualDSP++.

Note Profiling data gathered from a running program may be incorrect.

- 3 To view the profile report, enter the following command at the MATLAB command prompt:

```
profile(objectname, 'report')
```

where *objectname* is the name you provided in **IDE link handle name** in step 4 above and **report** is required to generate the profile report. MATLAB returns a graphic of the execution report and the HTML execution report. The following figure shows a sample profiling report graphic generated from the Code Generation Workflow Example (vdspworkf1ow1) demo.



Refer to profile for more information.

Functions — By Category

Constructor (p. 5-2)	adivdsp object constructor
File and Project Operations (p. 5-3)	Work with VisualDSP++ projects and sessions
IDDE Operations (p. 5-4)	Work with VisualDSP++
Processor Operations (p. 5-5)	Control processor
Debug Operations (p. 5-6)	Perform project and code debugging
Read/Write Operations (p. 5-7)	Access memory on the processor
Get Information Operations (p. 5-8)	Project and memory operations
Object Information (p. 5-9)	Object property information
Status Operations (p. 5-10)	Determine processor operation status
Session Operations (p. 5-11)	Manage VisualDSP++ sessions
Verification (p. 5-12)	Functions that help verify code performance

Constructor

adivdsp

Create object to session in
VisualDSP++ IDDE

File and Project Operations

activate	Make specified project, file, or configuration active
add	Add file or data type to active project
build	Build or rebuild current project
close	Close file in IDDE window
new	New text, project, or configuration file
open	Open specified file
remove	Remove file from active project in IDDE window
save	Save file

IDDE Operations

<code>cd</code>	Set IDDE working directory
<code>dir</code>	Files and directories in current IDDE window
<code>visible</code>	Visibility of IDDE window

Processor Operations

halt	Halt program execution by processor
load	Load file into processor
profile	Real-time task execution report
reset	Stop program execution and reset processor
run	Execute program loaded on processor

Debug Operations

delete

Remove breakpoint

insert

Insert breakpoint in file

Read/Write Operations

read

Read data from processor memory

write

Write data to processor memory
block

Get Information Operations

address

Return address and memory type of specified symbol

info

Property names and values for active session

Object Information

display

Properties of adivdsp object

Status Operations

`isrunning`

Determine whether processor is executing process

`isvisible`

Determine if IDDE is running on desktop and window is open

Session Operations

`listsessions`

List existing sessions

Verification

profile

Real-time task execution report

Functions — Alphabetical List

activate

Purpose Make specified project, file, or configuration active

Syntax

```
activate(vd, 'my_project.dpj', 'project')
activate(vd, 'my_file', 'text')
activate(vd, 'my_config', 'buildcfg')
```

Description `activate(vd, 'my_project.dpj', 'project')` uses handle `vd` to activate the project named `my_project.dpj` in the IDDE. If `my_project.dpj` does not exist in the IDDE, MATLAB issues an error that explains that the specified project does not exist.

VisualDSP++ IDDE allows you to have two or more projects with the same name open at the same time, such as `c:\try11\try11.dpj` and `c:\try12\try11.dpj`. If you use the following function to activate the project `try11.dpj` at the command prompt, where you do not provide the full path to the project:

```
activate(vd, 'try11.dpj')
```

Link for ADI VisualDSP++ cannot tell which project named `try11.dpj` to activate and may not activate the correct one. The following steps describe how Link for ADI VisualDSP++ decides which project to activate.

- 1** Search the current VisualDSP++ IDDE directory to find the first project with the specified name. If the search finds the project, Link for ADI VisualDSP++ activates the project and returns.
- 2** If the specified project is not found in the IDDE, search the MATLAB path to find a project with this name. If the search finds the project, Link for ADI VisualDSP++ activates the project and returns.
- 3** If Link for ADI VisualDSP++ search cannot find a project with the specified name in the VisualDSP++ IDDE or on the MATLAB path, the software returns an error saying it could not find the specified project.

`activate(vd, 'my_file', 'text')` If the document window is open, this command makes the file `my_file` active in the document window. If the document window is closed, MATLAB returns an error explaining that the document window is closed, and does not activate any file. If the specified file does not exist in the project, MATLAB returns an error. `activate` supports the text file extensions on the following list:

- `.txt`
- `.c`
- `.html`
- `.xml`

`activate(vd, 'my_config', 'buildcfg')` If the IDDE application is open, and it contains an active project, `activate` makes build configuration `my_config` the active configuration in the IDDE. Otherwise, MATLAB returns an error message stating that there is no active project and it could not activate the specified build configuration.

See Also

`new`

`remove`

add

Purpose Add file or data type to active project

Syntax `add(vd, 'my_file')`

Description `add(vd, 'my_file')` adds the file `my_file` to the active project from the current MATLAB working directory. If you do not have an active project in the IDDE, MATLAB returns an error message and does not add the file. You can specify the file by name, if the file is in your MATLAB or Link for Analog Devices VisualDSP++[®] working directory, or provide the fully qualified path to the file when the file is not in your working directories.

To add a file `add.txt` that is in your MATLAB working directory to the IDDE, use the following command:

```
add(vd, 'add.txt');
```

where `vd` is the handle for your `vdspink` object. If the file `add.txt` is not in either working directory, the command changes to include the full path to the file:

```
add(vd, 'fullpathtofile\add.txt');
```

You can add files of all types that the IDDE supports. The following table shows the supported file types.

Support File Type	File Extension
C/C++ source files	*.cpp, *.c, *.cxx, *.h, *.hpp, *.hxx
Assembly source files	*.asm, *.dsp
Object and Library files	*.doj, *.dlb
Linker Command files	*.ldf
VisualDSP++ support file	*.vdk

See Also

activate

cd

open

remove

address

Purpose Return address and memory type of specified symbol

Syntax `a=address(vd, 'symbolstring')`

Description `a=address(vd, 'symbolstring')` returns the address and memory type values for the symbol identified by `symbolstring`. For `address` to work, `symbolstring` must be a symbol in the symbol table for your active project. There must be a linker command file (`lcf`) in your project.

See Also `read`
`write`

Purpose

Create object to session in VisualDSP++ IDDE

Syntax

```
vd = adivdsp
vd = adivdsp('propname1',propvalue1,'propname2',
propvalue2,...,'timeout',value)
vd = adivdsp('my_session')
```

Description

vd = adivdsp opens the VisualDSP++ application for the most recent active session, if the IDDE is not running and creates an object vd that references the newly-opened session. If the IDDE is running, adivdsp returns object vd that connects to the active session in the IDDE.

adivdsp creates an interface between MATLAB and Analog Devices VisualDSP++. If this is the first time you have used adivdsp, you must supply a session name as an input argument (refer to the next syntax).

Note The output (left-hand argument) object name you provide for adivdsp cannot begin with an underscore, such as `_vd`.

vd = adivdsp('sessionname','name','procnum','number',...) returns an object handle vd that you use to interact with a processor in the IDDE from MATLAB.

You use the debug methods (refer to “Debug Operations” on page 5-6 for the methods available) with this object to access memory and control the execution of the processor. adivdsp also enables you to create an array of objects for a multiprocessor board, where each object refers to one processor on the board. When vd is an array of objects, any method called with vd as an input argument is sent sequentially to all processors connected to the adivdsp object. VisualDSP++ provides the communication between the IDDE and the processor.

Parameters that you pass as input arguments to adivdsp are interpreted as object property definitions. Each property definition consists of a property name followed by the desired property value (often called a PV, or property name/property value, pair). Although you

can define any `adivdsp` object property when you create the object, there are several important properties that you must provide during object construction. These properties must be properly delineated when you create the object. The required input arguments are

- `sessionname`—Specifies the session to connect to. This session must exist in the session list. `adivdsp` does not create new sessions. The resulting object refers to a processor in `sessionname`. To see the list of sessions, use `listsessions` at the MATLAB command prompt.
- `procnum`—Specifies the processor to connect to in `sessionname`. The default value for `procnum` is 0 for the first processor on the board. If you omit the `procnum` argument, `adivdsp` connects to the first processor. `procnum` can also be an array of processor indexes on a multiprocessor board. Using an array results in the `adivdsp` object `vd` being an array of handles that correspond to the specified processors.

After you build the `adivdsp` object `vd`, you can review the object property values with `get`, but you cannot modify the `sessionname` and `procnum` property values.

To connect to the active session in IDDE, omit the `sessionname` property in the syntax. If you do not pass `sessionname` as an input argument, the object defaults to the active session in the IDDE.

Use `listsessions` to determine the number for the desired DSP processor(s). If your IDDE session is single processor or to connect to processor zero, you can omit the `procnum` property definition. If `procnum` is not passed as an input argument, the object defaults to `procnum = 0` (zero-based).

`vd =`

`adivdsp('propname1',propvalue1,'propname2', propvalue2,...,'timeout',value)` sets the global time-out value to `value` in `vd`. MATLAB waits for the specified time-out value to get a response from the IDDE application. If the IDDE does not respond within the allotted time-out period, MATLAB exits from the evaluation of this function.

`vd = adivdsp('my_session')` connects to `my_session` if the session exists in the session list and the IDDE is not already running. In this case, MATLAB starts VisualDSP++ IDDE for the session named `my_session`.

The following list shows some other possible cases and results of using `adivdsp` to construct an object that refers to `my_session`.

- If `my_session` does not exist in the session list and the IDDE is not already running, MATLAB returns an error stating that `my_session` does not exist in the session list.
- When `my_session` is the current active session and the IDDE is already running, MATLAB connects to the IDDE for this session.
- If `my_session` is not the current active session, but exists in the session list, and the IDDE is already running, MATLAB displays a dialog box asking if you want to switch to `my_session`. If you choose to switch to `my_session`, all existing handles you have to other sessions in the IDDE become invalid. To connect to the other sessions you need to use `adivdsp` to recreate the objects for those sessions.
- If `my_session` does not exist in the session list and the IDDE is already running, MATLAB returns an error, explaining that the session `my_session` does not exist in the session list.

Examples

These examples demonstrate some of the operation of `adivdsp`.

```
vd = adivdsp('sessionname','my_session','procnum',0);
```

returns a handle to the first DSP processor for session `my_session`.

```
vd =  
adivdsp('sessionname','my_multiproc_session','procnum',[0  
1]);
```

returns a 1-by-2 array of handles to the first and second DSP processor for the multiprocessor session `my_multiproc_session`. `vd(1)` is the handle for first processor (0) `vd(2)` is the handle for second processor (1).

adivdsp

`vd = adivdsp` without input arguments constructs the object `vd` with the default property values, returning a handle to the first DSP processor for the active session in the IDDE.

`vd = adivdsp('sessionname', 'my_session');` returns a handle to the first DSP processor for the session `my_session`.

See Also

`listsessions`

Purpose Build or rebuild current project

Syntax

```
build(vd)
build(vd,timeout)
build(vd,'all')
build(vd,'all',timeout)
```

Description `build(vd)` incrementally builds the active project. Incremental builds recompile only source files in your project that you changed or added after the most recent build. `build` uses the file time stamp to determine whether to recompile a file. After recompiling the source files, `build` links the files to make a new program file.

`build(vd,timeout)` incrementally builds the active project with a time limit for how long MATLAB waits for the build process to complete. `timeout` defines the upper limit in seconds for the period the build routine waits for confirmation that the build process is finished. If the build process exceeds the time-out period, control returns to MATLAB immediately with a time-out error. Usually, `build` causes the processor to initiate a restart, even if it reaches the time-out limit. The time-out error in MATLAB indicates that confirmation was not received before the time-out period expired. The build action continues. Generally, the build and link process finishes successfully in spite of the time-out error.

`build(vd,'all')` rebuilds all the files in the active project.

`build(vd,'all',timeout)` rebuilds all the files in the active project applying the time-out limit on how long MATLAB waits for the build process to complete.

See Also

`isrunning`
`open`

cd

Purpose Set IDDE working directory

Syntax
`wd = cd(vd)`
`cd (vd, 'directory')`

Description `wd = cd(vd)` returns the current IDDE working directory, where `vd` is an `adivdsp` object that refers to the VisualDSP++ window, or a vector of objects.

`cd (vd, 'directory')` sets the IDDE working directory to 'directory'. 'directory' can be a path string relative to your current working directory, or an absolute path. The intended directory must exist. `cd` does not create a new directory. Setting the IDDE directory does not affect your MATLAB working directory.

`cd` alters the default directory for `open` and `load`. Loading a new workspace file also changes the working directory for the IDDE.

See Also
`dir`
`load`
`open`

Purpose

Close file in IDDE window

Syntax

```
close (vd, 'filename', 'filetype')
```

Description

`close (vd, 'filename', 'filetype')` closes the file named 'filename' in the active project in the vd IDDE window. If filename is not an open file in the IDDE, MATLAB returns a warning message. When you enter null value [] for filename, close closes the current active file in the IDDE. filename must match exactly the name of the file to close. If you enter all for the filename, close closes all files in the project that are of the type specified by filetype.

Note CLOSE does not save the file before closing it and it does not prompt you to save the file. You lose any changes you made after the most-recent save operation. Use save to ensure that your changes are preserved before you close the file.

The parameter 'filetype' is optional, with the default value of 'text'. Allowed 'filetype' strings are 'project', 'projectgroup', 'text', and 'workspace'. Here are some examples of close operation commands. In these examples, vd is an adivdsp object handle to the IDDE.

```
close(vd, 'all', 'project') — Closes all open project files
```

```
close(vd, 'my.dpj', 'project') — Closes the open project my.dpj
```

```
close(vd, [], 'project') — Closes the active open project
```

```
close(vd, 'all', 'projectgroup') — Close all open project groups
```

```
close(vd, 'myg.dpg', 'projectgroup') — Closes the project group  
myg.dpg
```

```
close(vd, [], 'projectgroup') — Closes the active project group
```

```
close(vd, 'all', 'text') — Close all text files
```

```
close(vd, 'text.c', 'text') — Closes the text file text.c
```

close

`close(vd,[], 'text')` — Closes the active text file

See Also

`add`

`open`

`save`

Purpose Remove breakpoint

Syntax

```
delete(vd,addr)
delete(vd,'filename','linenumber')
delete(vd,'all')
```

Description `delete(vd,addr)` removes a breakpoint located at the memory address `addr` of the processor. Provide the address input value in hexadecimal format, such as `0x244fc`, or `0x0014`.

`delete(vd,'filename','linenumber')` removes the breakpoint located at the line number `'linenumber'` in the file `'filename'` for the processor.

`delete(vd,'all')` removes all breakpoints in the current project source files.

See Also `insert`

dir

Purpose Files and directories in current IDDE window

Syntax `dir(vd)`
`d=dir(vd)`

Description `dir(vd)` lists the files and directories in the IDDE working directory, where `vd` is the handle to the IDDE. `vd` can be either a single handle, or a vector of handles. When `vd` is a vector, `dir` returns the files and directories for each handle.

`d=dir(vd)` returns the list of files and directories as an M-by-1 structure in `d` with the following fields for each file and directory, as shown in the following table.

Field Name	Description
<code>name</code>	Name of the file or directory.
<code>date</code>	Date of most recent file or directory modification.
<code>bytes</code>	Size of the file in bytes. Directories return 0 for the number of bytes.
<code>isdirectory</code>	0 if this is a file, 1 if this is a directory.

To view the entries in `d`, use an index in the command at the MATLAB prompt, as shown by the following examples.

- `d(3)` returns the third element in the structure.
- `d(10)` returns the tenth element in the structure `d`.
- `d(4).date` returns the date field value for the fourth structure element.

See Also `cd`
`open`

Purpose Properties of adivdsp object

Syntax `display(vd)`

Description `display(vd)` displays the properties and property values of the adivdsp object `vd`.

For example, when you create `vd` associated with the session `Testsession` and the processor is the ADSP-BF533, `display(vd)` returns the following information in the MATLAB command window:

```
display(vd)
```

```
ADIVDSP Object:
```

```
Session name      : Testsession
Processor name    : ADSP-BF533
Processor type    : ADSP-BF533
Processor number  : 0
Default timeout   : 10.00 secs
```

See Also `get` in the MATLAB Function Reference

halt

Purpose Halt program execution by processor

Syntax `halt(vd)`
`halt(vd,timeout)`

Description `halt(vd)` stops the program running on the processor. After you issue this command, MATLAB waits for a response from the processor that the processor has stopped. By default, the wait time is 10 seconds. If 10 seconds elapses before the response arrives, MATLAB returns an error. In this syntax, the time-out period defaults to the global time-out period specified in `vd`. Use `get(vd, 'timeout')` to determine the global time-out period. However, the processor usually stops in spite of the error message.

To resume processing after you halt the processor, use `run`. Also, the `read(vd, 'pc')` function can determine the memory address where the processor stopped after you use `halt`.

`halt(vd,timeout)` immediately stops program execution by the processor. After the processor stops, `halt` returns to the host. `timeout` defines, in seconds, how long the host waits for the processor to stop running.

`timeout` defines the maximum time the routine waits for the processor to stop. If the processor does not stop within the specified time-out period, the routine returns with a time-out error.

Examples

Use one of the provided demonstration programs to show how `halt` works. From the VisualDSP++ demonstration programs, load and run one of the demonstration projects.

At the MATLAB prompt, create an object that refers to VisualDSP++

```
vd = adivdsp
```

Check whether the program is running on the processor.

```
isrunning(vd)
```

```
ans =  
  
    1  
  
vd.isrunning % Alternate syntax for checking the run status.  
  
ans =  
  
    1  
halt(vd) % Stop the running application on the processor.  
isrunning(vd)  
  
ans =  
  
    0
```

Issuing the `halt` stops the process on the processor. Checking in VisualDSP++ confirms that the process has stopped.

See Also

```
isrunning  
reset  
run
```

info

Purpose Property names and values for active session

Syntax `objinfo=info(vd)`

Description `objinfo=info(vd)` returns the property names and values associated with the active session and the processors for that session. The following table shows the properties `info` returns for `vd` and provides brief descriptions of the properties.

Property Name	Data Type	Description
<code>procname</code>	String	Provides the name of the processor.
<code>proctype</code>	String	Provide the platform name the session uses.
<code>revision</code>	String	Reports the silicon revision of the processor. Does not apply to simulators.

Examples

When you have an `adivdsp` object `vd`, `info` provides information about the object.

```
vd=adivdsp('sessionname','Testsession')
```

```
ADIVDSP Object:
```

```
Session name      : Testsession
Processor name    : ADSP-BF533
Processor type    : ADSP-BF533
Processor number  : 0
Default timeout   : 10.00 secs
```

```
objinfo=info(vd)
```

```
objinfo =
```

```
procname: 'ADSP-BF533'
proctype: 'ADSP-BF533'
```

```
revision: ''
```

```
objinfo.procname
```

```
ans =
```

```
ADSP-BF533
```

See Also

```
display
```

```
adivdsp
```

insert

Purpose Insert breakpoint in file

Syntax `insert(vd,addr)`
`insert(vd,'filename','linenumber')`

Description `insert(vd,addr)` inserts a breakpoint at the memory address specified by the `addr` parameter. `vd` identifies the session that adds the breakpoint.

`insert(vd,'filename','linenumber')` inserts a breakpoint at the line '`linenumber`' in the file '`filename`'.

See Also `address`
`delete`
`run`

Purpose Determine whether processor is executing process

Syntax `isrunning(vd)`

Description `isrunning(vd)` returns 1 when the processor is executing a program. When the processor is halted, `isrunning` returns 0.

Examples `isrunning` lets you determine whether the processor is running. After you load a program to the processor, use `isrunning` to verify that the program is running.

```
vd=adivdsp
```

```
ADIVDSP Object:
```

```
Session name      : Testsession
```

```
Processor name    : ADSP-BF533
```

```
Processor type    : ADSP-BF533
```

```
Processor number  : 0
```

```
Default timeout   : 10.00 secs
```

```
visible(vd,1)
```

```
load(vd, 'adi.dxe', 'program')
```

```
run(vd)
```

```
isrunning(vd)
```

```
ans =
```

```
1
```

```
halt(vd)
```

```
isrunning(vd)
```

```
ans =
```

```
0
```

isrunning

See Also

halt

load

run

Purpose	Determine if IDDE is running on desktop and window is open
Syntax	<code>isvisible(vd)</code>
Description	<code>isvisible(vd)</code> determines whether the VisualDSP++ IDDE is running on the desktop and the window is open. <code>isvisible</code> returns either 1 indicating that the IDDE is running and the window is open, or 0 indicating that either the IDDE is running in the background or is not running.
See Also	<code>visible</code>

listsessions

Purpose

List existing sessions

Syntax

```
list = listsessions
list = listsessions('verbose')
```

Description

`list = listsessions` returns `list` that contains a listing of all of the sessions by name currently in the development environment.

`list = listsessions('verbose')` adds the optional input argument `verbose`. When you include the `verbose` argument, `listsessions` returns a cell array that contains one row for each existing session. Each row has three columns — processor type, platform name, and processor name.

See Also

`adivdsp`

Purpose Load file into processor

Syntax `load(vd, 'filename', timeout)`
`load(, timeout)`

Description `load(vd, 'filename', timeout)` transfers file 'my_file.dxe' to the processor. `filename` can include a full path to the file, or the name of a file that is in the current working directory of VisualDSP++. Use the function `cd` to check or modify the VisualDSP++ working directory. Use this function only with program files that you created by a VisualDSP++ build process. When you issue the `load` command, the command waits for the period defined by `timeout` in `vd` for the process to complete—ten seconds.

`load(, timeout)` adds the optional parameter `timeout` that defines how long, in seconds, MATLAB waits for the specified load process to complete. If the time-out period expires before the load process returns a completion message, MATLAB generates an error and returns. Usually the program load process works correctly in spite of the error message.

See Also `cd`
`dir`
`open`

new

Purpose New text, project, or configuration file

Syntax `new(vd, 'name', 'type')`

Description `new(vd, 'name', 'type')` creates a new file, project, or build configuration in the active project. Input argument `name` specifies the name assigned to identify the new file, project, or configuration.

When you are creating a new file or project, `name` is a filename that can include the full path to the new file. If you omit the path, `new` creates the new file or project in your current VisualDSP++ working directory.

To define the kind of entity to create, `type` accepts the strings shown in the following table.

Type String	Description
text	Create an empty text file in the current session.
project	Create a new executable project in the current session. Sometimes this is called a <i>DSP executable file</i> .
projectlib	Create a new library project in the current session.
buildcfg	Create a build configuration in the active project.

Examples `new(vd, 'my_project.dpj', 'project', project_type)` creates a new project 'my_project.dpj' of type `project_type`. The `project_type` argument is optional; the default project type is DSP executable file.

`new(vd, 'my_config', 'buildcfg')` creates a new build configuration, named `my_config`, in the active project.

See Also `activate`

`close`

save

open

Purpose Open specified file

Syntax `open(vd, 'filename')`
`open(, 'filetype')`

Description `open(vd, 'filename')` opens file `filename` in the IDDE. If you specify the file extension in `filename`, `open` opens the file of that type. If you omit the file extension from the name, `open` assumes the file to open is a text file. The following table presents the possible file types and extensions.

File Type	Extension	Description
text	txt, c, asm, cpp, h, and all file extensions not listed elsewhere in this table	Normal text file
project	dpj	VisualDSP++
projectgroup	dpg	Project group in VisualDSP++
workspace	TBD	Workspace in VisualDSP++

If the file to open does not exist in the current project or directory path, MATLAB returns a warning and returns control to MATLAB.

`open(, 'filetype')` identifies the type of file to open. This can be useful when your project includes files of different types that have the same name or when you want to open a project, project group, or workspace. Using the input argument `filetype` overrides the file type defined by the file extension in the file name. The preceding table defines the valid file type extensions.

`open(, timeout)` adds the optional parameter `timeout` that defines how long, in seconds, MATLAB waits for the specified load process to complete. If the time-out period expires before the load process returns a completion message, MATLAB returns an error. Usually the program load process works correctly in spite of the error message.

See Also

cd
dir
load
new

profile

Purpose Real-time task execution report

Syntax `profile(vd, 'report')`

Description `profile(vd, 'report')` returns the real-time task execution profile report in HTML and graphical plot forms. The **report** input argument is required. When you select the **Profile real-time task execution** option in the configuration parameters for your model, and then build and run your model on a processor, this function accesses the report of the process execution.

Note Real-time task execution profiling works with hardware only. Simulators do not support the profiling feature.

The HTML report contains the sections described in the following table.

Section Heading	Description
Worst case task turnaround times	Maximum task turnaround time for each task since model execution started.
Maximum number of concurrent overruns for each task	Maximum number of concurrent task overruns since model execution started.
Analysis of profiling data recorded over <i>nnn</i> seconds.	Profiling data was recorded over <i>nnn</i> seconds. The recorded data for task turnaround times and task execution times is presented in the table below this heading.

Task turnaround time is the elapsed time between starting and finishing the task. If the task is not preempted, task turnaround time equals the task execution time.

Task execution time is the time between task start and finish when the task is actually running. It does not include time during which the task may have been preempted by another task.

Note Task execution time cannot be measured directly. Task profiling infers the execution time from the task start and finish times, and the intervening periods during which the task was preempted by another task.

The execution time calculations do not account for processor time consumed by the scheduler while switching tasks. In cases where preemption occurs, the reported task execution times overestimate the true task execution time.

Task overruns occur when a timer task does not complete before the same task is scheduled to run again. Depending on how you configure the real-time scheduler, a task overrun may be handled as a real-time failure. Alternatively, you might allow a small number of task overruns to accommodate cases where a task occasionally takes longer than normal to complete. If a task overrun occurs, and the same task is scheduled to run again before the first overrun has been cleared, concurrent task overruns are said to have occurred.

Here is a sample of the HTML profiling report—task execution profile report.

See Also

load

run

read

Purpose Read data from processor memory

Syntax

```
mem = read(vd, address)
mem = read(..., datatype)
mem = read(..., count)
mem = read(..., memorytype)
mem = read(..., timeout)
```

Description `mem = read(vd, address)` returns a block of data values from the memory space of the DSP processor referenced by `vd`. The block to read begins from the DSP memory location given by the input parameter `address`. The data is read starting from `address` without regard to type-alignment boundaries in the DSP. Conversely, the byte ordering defined by the data type is automatically applied.

`address` is a decimal or hexadecimal representation of a memory address in the DSP. In all cases, the full memory address consist of two parts:

- The start address
- The memory type

You can use a numeric vector representation of the address (see below) to define the memory type value explicitly .

Alternatively, the `vd` object has a default memory type value that is applied when the memory type value is not explicitly incorporated in the passed address parameter. In DSP processors with only a single memory type, it is possible to specify all addresses using the abbreviated (implied memory type) format by setting the `vd` object memory type value to zero.

Note You cannot read data from processor memory while the processor is running.

Provide the address parameter either as a numerical value that is a decimal representation of the DSP memory address, or as a string that read converts to the decimal representation of the start address. (Refer to function `hex2dec` in the MATLAB Function Reference. `read` uses `hex2dec` to convert the hexadecimal string to a decimal value).

The examples in the following table demonstrate how `read` uses the address parameter:

address Parameter Value	Description
131082	Decimal address specification. The memory start address is 131082 and memory type is 0. This is the same as specifying [131082 0].
[131082 1]	Decimal address specification. The memory start address is 131082 and memory type is 1.
'2000A'	Hexadecimal address specification provided as a string entry. The memory start address is 131082 (converted to the decimal equivalent) and memory type is 0.

It is possible to specify address as a cell array. You can use a combination of numbers and strings for the start address and memory type values. For example, the following are valid addresses from cell array `myaddress`:

```
myaddress1 myaddress1{1} = 131072; myaddress1{2} =
'Program(PM) Memory';
```

```
myaddress2 myaddress2{1} = '20000'; myaddress2{2} =
'Program(PM) Memory';
```

```
myaddress3 myaddress3{1} = 131072; myaddress3{2} = 0;
```

`mem = read(..., datatype)` where the input argument `datatype` defines the interpretation of the raw values read from DSP memory. Parameter `datatype` specifies the data format of the raw memory image. The data is read starting from address without regard to data type alignment

boundaries in the DSP. The byte ordering defined by the data type is automatically applied. This syntax supports the following MATLAB data types:

MATLAB Data Type	Description
double	IEEE double-precision floating point value
single	IEEE single-precision floating point value
uint8	8-bit unsigned binary integer value
uint16	16-bit unsigned binary integer value
uint32	32-bit unsigned binary integer value
int8	8-bit signed two's complement integer value
int16	16-bit signed two's complement integer value
int32	32-bit signed two's complement integer value

`read` does not coerce data type alignment. Some combinations of address and datatype will be difficult for the processor to use.

`mem = read(...,count)` adds the `count` input parameter that defines the dimensions of the returned data block `mem`. To read a block of multiple data values, specify `count` to determine how many values to read from address. `count` can be a scalar value that causes `read` to return a column vector that has `count` values. You can perform multidimensional reads by passing a vector for `count`. The elements in the input vector of `count` define the dimensions of the returned data matrix. The memory is read in column-major order. `count` defines the

dimensions of the returned data array `mem` as shown in the following table.

- `n` — Read `n` values into a column vector.
- `[m,n]` — Read `m`-by-`n` values into `m` by `n` matrix in column-major order.
- `[m,n,...]` — Read a multidimensional matrix `m`-by-`n`-by...of values into an `m`-by-`n`-by...array.

To read a block of multiple data values, specify the input argument count that determines how many values to read from address.

`mem = read(...,memorytype)` adds an optional input argument `memorytype`. Object `vd` has a default memory type value 0 that `read` applies if the memory type value is not explicitly incorporated into the passed address parameter.

In processors with only a single memory type, it is possible to specify all addresses using the implied memory type format by setting the `vd` `memorytype` property value to zero. Blackfin and SHARC use different memory types. Blackfin processors have one memory type. SHARC processors provide five types. The following table shows the memory types for both processor families.

String Entry for <code>memorytype</code>	Numerical Entry for <code>memorytype</code>	Processor Support
'program(pm) memory'	0	Blackfin and SHARC
'data(dm) memory'	1	SHARC
'data(dm) short word memory'	2	SHARC
'external data(dm) byte memory'	3	SHARC
'boot(prom) memory'	4	SHARC

read

`mem = read(...,timeout)` adds the optional parameter `timeout` that defines how long, in seconds, MATLAB waits for the specified read process to complete. If the time-out period expires before the read process returns a completion message, MATLAB returns an error and returns control to the MATLAB command prompt. Usually the read process works correctly in spite of the error message.

Examples

This example reads one 16-bit integer from memory on the processor.

```
mlvar = read(vd,131072,'int16')
```

131072 is the decimal address of the data to read.

You can read more than one value at a time. This read command returns 100 32-bit integers from the address 0x20000 and plots the result in MATLAB.

```
data = read(vd,'20000','int32',100)
plot(double(data))
```

See Also

`write`

Purpose Remove file from active project in IDDE window

Syntax `remove(vd, 'filename', 'filetype')`

Description `remove(vd, 'filename', 'filetype')` removes the file named `filename` from the active project in the `vd` window of the IDDE. If the file does not exist, MATLAB returns a warning and does not remove any files. The `filetype` argument is optional, with the default value of `text`. Possible values for `filetype` are: `project` and `text`.

See Also

- `add`
- `cd`
- `open`

reset

Purpose Stop program execution and reset processor

Syntax `reset(vd,timeout)`

Description `reset(vd,timeout)` stops the program executing on the processor and asynchronously performs a processor reset, returning all processor register contents to their power-up settings. `reset` returns immediately after the processor halt.

The `timeout` is an optional parameter, with the default value set to the global default value. The `timeout` determines how long, in seconds, MATLAB waits for the processor to halt.

See Also

- `halt`
- `load`
- `run`

Purpose Execute program loaded on processor

Syntax

```
run(vd)
run(vd, 'runopt')
run(..., timeout)
```

Description `run(vd)` runs the program file loaded on the referenced processor, returning immediately after the processor starts running. Program execution starts from the location of program counter (PC). Usually, the PC is positioned at the top of the executable file. However, if you stopped a running program with `halt`, the PC may be anywhere in the program. `run` starts the program from the PC current location.

If `vd` references more than one processor, each processor calls `run` in sequence.

`run(vd, 'runopt')` includes the parameter `runopt` that defines the action of the `run` method. The options for `runopt` are listed in the following table.

runopt string	Description
<code>run</code>	Executes the run and waits to confirm that the processor is running, and then returns to MATLAB.
<code>runtohalt</code>	Executes the run but then waits until the processor halts before returning. The halt can be the result of the PC reaching a breakpoint, or by direct interaction with VisualDSP++, or by the normal program exit process.

`run(..., timeout)` adds input argument `timeout`, to allow you to set the time-out to a value different from the global time-out value. The `timeout` value specifies how long, in seconds, MATLAB waits for the processor to start executing the loaded program before returning.

Most often, the `run` and `runtohalt` options cause the processor to initiate execution, even when a time-out is reached. The time-out

run

indicates that the confirmation was not received before the time-out period elapsed.

See Also

halt

load

reset

Purpose Save file

Syntax
`save(vd, 'filename')`
`save(vd, 'filename', 'filetype')`

Description `save(vd, 'filename')` saves the file named `filename` in VisualDSP++. `filename` must match the name of the file to save and you must include the file extension. You can save only open files. If you specify the `filename` parameter as `all`, every open file of the defined type is saved (refer to the `filetype` parameter in the next syntax). A null input, `[]`, for `filename` or no file name saves the current active file (the file that has focus).

`save(vd, 'filename', 'filetype')` saves the specified file in VisualDSP++.

`filetype` defines the type of file to save. In the following table you see examples of `save` that use the allowed file type definitions—`project`, `projectgroup`, and `text`.

save Command	Description of save Operation
<code>save(vd, 'all', 'project')</code>	Saves all project files
<code>save(vd, 'my.dpj', 'project')</code>	Saves the project <code>my.dpj</code>
<code>save(vd, [], 'project')</code>	Saves the active project
<code>save(vd, 'all', 'projectgroup')</code>	Saves all project files in the project groups
<code>save(vd, 'myg.dpg', 'projectgroup')</code>	Saves the project group <code>myg.dpg</code>
<code>save(vd, [], 'projectgroup')</code>	Saves the projects in the active project group
<code>save(vd, 'all', 'text')</code>	Save all text files

save

save Command	Description of save Operation
<code>save(vd, 'text.c', 'text')</code>	Saves the text file <code>text.c</code>
<code>save(vd, [], 'text')</code>	Save the active text file

See Also

`adivdsp`

`close`

`load`

Purpose Visibility of IDDE window

Syntax `visible(vd, state)`

Description `visible(vd, state)` sets the visibility state of the IDDE window defined by `vd`. Possible values of `state` are 0 for not visible, and 1 for visible. Setting the state to 1 forces the IDDE to be visible on the desktop so you can interact directly with it. Setting to 0 hides the IDDE—the IDDE runs in the background. In the not visible state, you interact with the IDDE from the MATLAB command line. When you create an `adivdsp` object, the IDDE visibility is set to 0 and the IDDE is not visible.

See Also `info`
`isvisible`

write

Purpose Write data to processor memory block

Syntax

```
mem = write(vd, address, data)
mem = write(..., datatype)
mem = write(..., memorytype)
mem = write(..., timeout)
```

Description `mem = write(vd, address, data)` writes data, a collection of values, to the memory space of the DSP processor referenced by `vd`. Input argument `data` is a scalar, vector or array of values to write to the memory of the processor. The block to write begins from the DSP memory location given by the input parameter `address`.

The data is written starting from `address` without regard to type-alignment boundaries in the DSP. Conversely, the byte ordering of the data type is automatically applied.

Note You cannot write data to processor memory while the processor is running.

`address` is a decimal or hexadecimal representation of a memory address in the processor. In all cases, the full memory address consist of two parts: the start address and the memory type. The memory type value can be explicitly defined using a numeric vector representation of the address (see below).

Alternatively, the `vd` object has a default memory type value which is applied if the memory type value is not explicitly incorporated into the passed address parameter. In DSP processors with only a single memory type, by setting the `vd` object memory type value to zero it is possible to specify all addresses using the abbreviated (implied memory type) format.

You provide the address parameter either as a numerical value that is a decimal representation of the DSP memory address, or as a string that `write` converts to the decimal representation of the start address.

(Refer to function `hex2dec` in the MATLAB Function Reference that `read` uses to convert the hexadecimal string to a decimal value).

To demonstrate how `write` uses `address`, here are some examples of the `address` parameter:

address Parameter Value	Description
131082	Decimal address specification. The memory start address is 131082 and memory type is 0. This is the same as specifying [131082 0].
[131082 1]	Decimal address specification. The memory start address is 131082 and memory type is 1.
'2000A'	Hexadecimal address specification provided as a string entry. The memory start address is 131082 (converted to the decimal equivalent) and memory type is 0.

It is possible to specify `address` as a cell array, in which case you can use a combination of numbers and strings for the start address and memory type values. For example, the following are valid addresses from cell array `myaddress`:

```
myaddress1 myaddress1{1} = 131072; myaddress1{2} =
'Program(PM) Memory';
```

```
myaddress2 myaddress2{1} = '20000'; myaddress2{2} =
'Program(PM) Memory';
```

```
myaddress3 myaddress3{1} = 131072; myaddress3{2} = 0;
```

`mem = write(...,datatype)` where the input argument `datatype` defines the interpretation of the raw values written to DSP memory. Parameter `datatype` specifies the data format of the raw memory image. The data is written starting from `address` without regard to data type alignment boundaries in the DSP. The byte ordering of the data type is automatically applied. The following MATLAB data types are supported:

write

MATLAB Data Type	Description
double	IEEE double-precision floating point value
single	IEEE single-precision floating point value
uint8	8-bit unsigned binary integer value
uint16	16-bit unsigned binary integer value
uint32	32-bit unsigned binary integer value
int8	8-bit signed two's complement integer value
int16	16-bit signed two's complement integer value
int32	32-bit signed two's complement integer value

`write` does not coerce data type alignment. Some combinations of address and datatype will be difficult for the processor to use.

`mem = write(...,memorytype)` adds an optional input argument `memorytype`. Object `vd` has a default memory type value 0 that `write` applies if the memory type value is not explicitly incorporated into the passed address parameter. In processors with only a single memory type, it is possible to specify all addresses using the implied memory type format by setting the `vd` `memorytype` property value to zero.

Blackfin and SHARC use different memory types. Blackfin processors have one memory type. SHARC processors provide five types. The following table shows the memory types for both processor families.

String Entry for memorytype	Numerical Entry for memorytype	Processor Support
'program(pm) memory'	0	Blackfin and SHARC
'data(dm) memory'	1	SHARC
'data(dm) short word memory'	2	SHARC
'external data(dm) byte memory'	3	SHARC
'boot(prom) memory'	4	SHARC

`mem = write(...,timeout)` adds the optional parameter `timeout` that defines how long, in seconds, MATLAB waits for the specified write process to complete. If the timeout period expires before the write process returns a completion message, MATLAB displays an error and returns control to the command prompt. Usually the process works correctly in spite of the error message.

Examples

These three syntax examples demonstrate how to use `write` in some common ways. In the first example, write an array of 16-bit integers to location `[131072 1]`.

```
write(vd,[131072 1],int16([1:100]));
```

Now write a single-precision IEEE floating point value (32-bits) at address `2000A`(Hex).

```
write(vd,'2000A',single(23.5));
```

For the third example, write a 2-D array of integers in row-major format (standard C programming format) at address `131072` (decimal).

```
mlarr = int32([1:10;101:110]);
```

write

```
write(vd,131072,mlarr);
```

See Also

[hex2dec](#) in the MATLAB Function Reference

[read](#)

Blocks — By Category

Blackfin DSP Support (p. 7-2)

Work with Blackfin processors

Core Support (p. 7-3)

Work with Analog Devices processors

SHARC DSP Support (p. 7-4)

Work with SHARC processors

TigerSHARC DSP Support (p. 7-5)

Work with TigerSHARC processors

Blackfin DSP Support

Blackfin Hardware Interrupt

Target Preferences

Generate Interrupt Service Routine

Configure model for Analog Devices
processor

Core Support

Idle Task

Memory Allocate

Memory Copy

Create free-running task

Allocate memory section on Blackfin,
SHARC, TigerSHARC processors

Copy to and from memory section

SHARC DSP Support

SHARC Hardware Interrupt
Target Preferences

Generate Interrupt Service Routine
Configure model for Analog Devices
processor

TigerSHARC DSP Support

Target Preferences

Configure model for Analog Devices
processor

TigerSHARC Hardware Interrupt

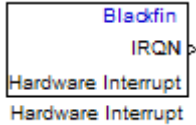
Generate Interrupt Service Routine

Blocks — Alphabetical List

Blackfin Hardware Interrupt

Purpose Generate Interrupt Service Routine

Library Blackfin DSP Support in Link for Analog Devices VisualDSP++®



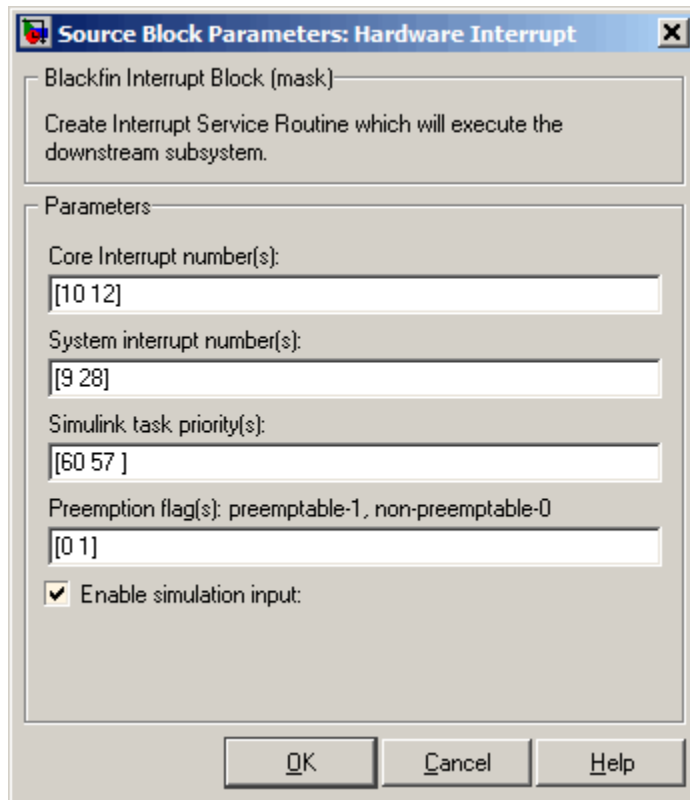
Description Create interrupt service routines (ISR) in the software generated by the build process. When you incorporate this block in your model, code generation results in ISRs on the processor that run the processes that are downstream from the this block or an Idle Task block connected to this block. Core interrupts trigger the ISRs. System interrupts trigger the core interrupts. In the following figure, you see the mapping possibilities between system interrupts and core interrupts.

Interrupts

Blackfin processors support the interrupt numbers shown in the following table. Some Blackfin processors do not support all of the system interrupts.

Interrupt Description	Valid Range in Link for ADI VisualDSP++
Core interrupt numbers	7 to 15
System interrupt numbers	0 to 31 (The upper end value depends on the processor. May be less than 31.)

Dialog Box



Core interrupt number(s)

Specify a vector of one or more interrupt numbers for the interrupt service routines (ISR) to install. The valid range is 7 to 15, where 7 through 13 are hardware driven, and 14 and 15 are software driven. Core interrupts numbered 0 to 6 are reserved and cannot be entered in this field.

The width of the block output signal corresponds to the number of interrupt values you specify in this field. Triggering of each ISR depends on the core interrupt value, the system interrupt value, and the preemption flag you enter for each interrupt. These three

Blackfin Hardware Interrupt

values define how the code and processor respond to interrupts during asynchronous scheduler operations.

System interrupt number(s)

System interrupt numbers identify system interrupts to map to core interrupts. Enter one or more values as a vector. The valid range is 0 through 31, although the valid range depends on your processor. Some processors do not support the full range of 32 system interrupts. Link for ADI VisualDSP++ does not test for valid system interrupt values. You must verify that your values are valid for your processor. You must specify at least one system interrupt number to use asynchronous scheduling.

The block maps the first interrupt value in this field to the first core interrupt value you enter in **Core interrupt number(s)**, it maps the second system interrupt value to the second core interrupt value, and so on until it has mapped all of the system interrupt values to core interrupt values. You cannot map more than one system interrupt to the same core interrupt. Therefore, you can enter one system interrupt value in this field and map it to more than one core interrupt. You cannot enter more than one value in this field and map the values to one core interrupt.

When you trigger one of the system interrupts in this field, the block triggers the ISR associated with the core interrupt that is mapped to the system interrupt.

Simulink task priority(s)

Each output of the Hardware Interrupt block drives a downstream block (for example, a function call subsystem). Simulink task priority specifies the Simulink priority of the downstream blocks. Specify an array of priorities corresponding to the interrupt numbers entered in **Interrupt number(s)**.

Proper code generation requires rate transition code (see Rate Transitions and Asynchronous Blocks). The task priority values ensure absolute time integrity when the asynchronous task must obtain real time from its base rate or its caller. Typically, assign

priorities for these asynchronous tasks that are higher than the priorities assigned to periodic tasks.

Preemption flag(s) preemptable – 1, non-preemptable – 0

Higher priority interrupts can preempt interrupts that have lower priority. To control this preemption, use the preemption flags to specify whether an interrupt can be preempted.

- Entering 1 indicates the corresponding core interrupt can be preempted.
- Entering 0 indicates the corresponding interrupt cannot be preempted.

When **Core interrupt numbers** contains more than one interrupt priority, you can assign different preemption flags to each interrupt by entering a vector of preemption flag values that correspond to the order of the interrupts in **Core interrupt numbers**. If **Core interrupt numbers** contains more than one interrupt, and you enter only one flag value in this field, that status applies to all interrupts.

For example, the default settings [0 1] indicate that the interrupt with value 10 in **Core interrupt numbers** is not preemptible and the value 12 interrupt can be preempted.

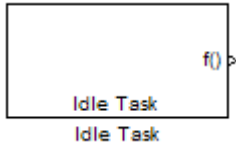
Enable simulation input

When you select this option, Simulink adds an input port to the Hardware Interrupt block. This port receives input only during simulation. Connect one or more simulated interrupt sources to the simulation input.

Idle Task

Purpose Create free-running task

Library DSP Core Support in Link for Analog Devices VisualDSP++®



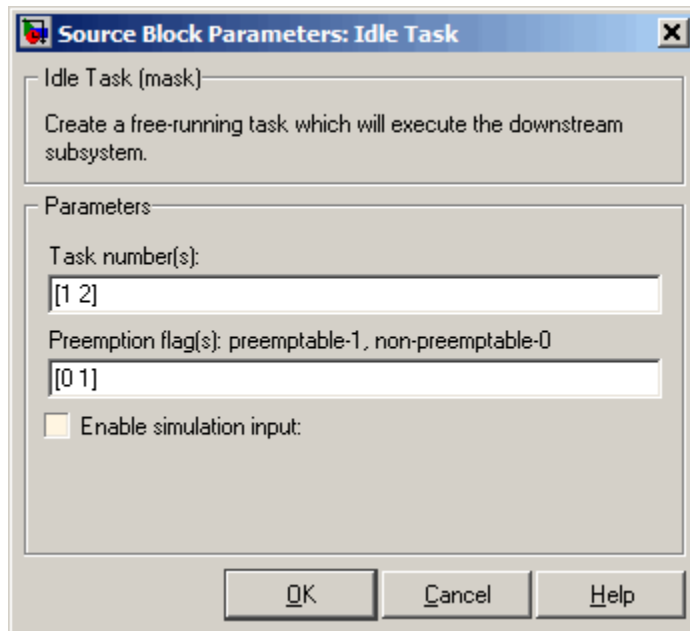
Description The Idle Task block, and the subsystem connected to it, specify one or more functions to execute as background tasks. All tasks executed through the Idle Task block are of the lowest priority, lower than that of the base-rate task.

Vectorized Output

The block output comprises a set of vectors—the task numbers vector and the preemption flag or flags vector. Any preemption flag vector must be the same length as the number of tasks vector unless the preemption flag vector has only one element. The value of the preemption flag determines whether a given interrupt (and corresponding task) is preemptible. Preemption overrides prioritization. A lower-priority, nonpreemptible task can preempt a higher-priority, preemptible task.

When the preemption flag vector has only one element, that element value applies to all functions in the downstream subsystem as defined by the task numbers in the task number vector. If the preemption flag vector has the same number of elements as the task number vector, each task defined in the task number vector has a preemption status defined by the value of the corresponding element in the preemption flag vector.

Dialog Box



Task number(s)

Identifies the created tasks by number. Enter as many tasks as you need by entering a vector of integers. The default values are [1, 2], to indicate that the downstream subsystem has two functions.

The values you enter determine the execution order of the functions in the downstream subsystem, while the number of values you enter corresponds to the number of functions in the downstream subsystem.

Enter a vector containing the same number of elements as the number of functions in the downstream subsystem. This vector can contain no more than 16 elements, and the values must be from 0 to 15 inclusive.

Idle Task

The value of the first element in the vector determines the order in which the first function in the subsystem is executed. Similarly, the value of the second element determines the order in which the second function in the subsystem is executed, and so on.

For example, entering the vector [2,3,1] in this field indicates that there are three functions to be executed, and that the third function is executed first, the first function is executed second, and the second function is executed third. After all functions are executed, the Idle Task block cycles back and repeats the execution of the functions in the same order.

Preemption flag(s)

Higher-priority interrupts can preempt interrupts that have lower priority. To allow you to control preemption, use the preemption flags to specify whether an interrupt can be preempted.

- Entering 1 indicates that the interrupt can be preempted.
- Entering 0 indicates the interrupt cannot be preempted.

When **Task number(s)** contains more than one task, you can assign different preemption flags to each task by entering a vector of flag values, corresponding to the order of the tasks in **Task number(s)**. If **Task number(s)** contains more than one task, and you enter only one flag value in this field, that preemption setting applies to all tasks.

For example, the default settings [0 1] indicate the task with priority 1 in **Task number(s)** is not preemptible, and the priority 2 task can be preempted.

Enable simulation input

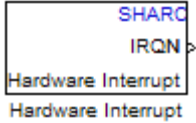
When you select this option, Simulink adds an input port to the Idle Task block. This port receives input only during simulation. Connect one or more simulated interrupt sources to the simulation input.

Note Select this check box to test asynchronous interrupt processing behavior in Simulink.

SHARC Hardware Interrupt

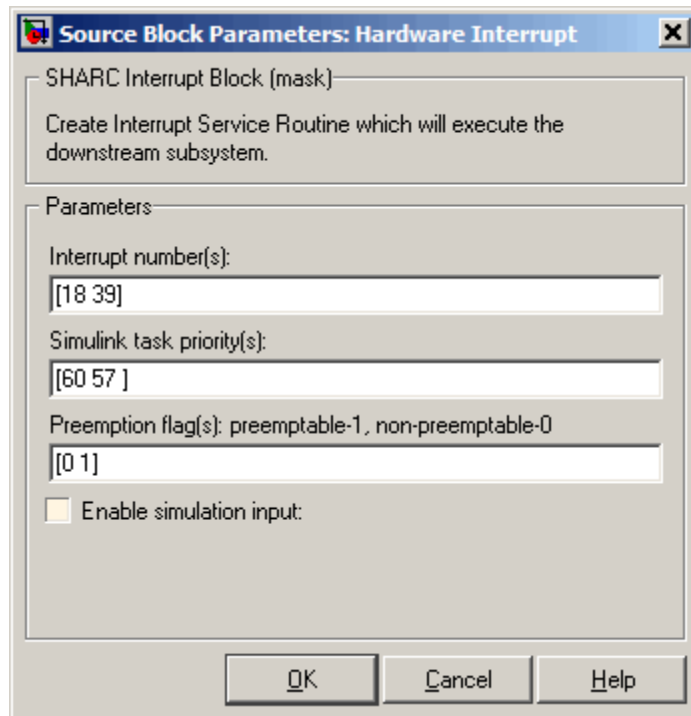
Purpose Generate Interrupt Service Routine

Library SHARC DSP Support in Link for Analog Devices VisualDSP++®



Description Create interrupt service routines (ISR) in the software generated by the build process. When you incorporate this block in your model, code generation results in ISRs on the processor that either run the processes that are downstream from this block or trigger an Idle Task block connected to this block.

Dialog Box



Interrupt number(s)

Specify an array of interrupt numbers for the interrupts to install. The valid range is 0 to 99.

The width of the block output signal corresponds to the number of interrupt numbers specified in this field. The values in this field and the preemption flag entries in **Preemption flag(s): preemptable-1, non-preemptable-0** define how the code and processor handle interrupts during asynchronous scheduler operations.

Simulink task priority(s)

Each output of the Hardware Interrupt block drives a downstream block (for example, a function call subsystem). Simulink task

SHARC Hardware Interrupt

priority specifies the Simulink priority of the downstream blocks. Specify an array of priorities corresponding to the interrupt numbers entered in **Interrupt number(s)**.

Proper code generation requires rate transition code (see Rate Transitions and Asynchronous Blocks). The task priority values ensure absolute time integrity when the asynchronous task must obtain real time from its base rate or its caller. Typically, assign priorities for these asynchronous tasks that are higher than the priorities assigned to periodic tasks.

Preemption flag(s) preemptable – 1, non-preemptable – 0

Higher-priority interrupts can preempt interrupts that have lower priority. To allow you to control preemption, use the preemption flags to specify whether an interrupt can be preempted.

- Entering 1 indicates that the interrupt can be preempted.
- Entering 0 indicates the interrupt cannot be preempted.

When **Interrupt numbers** contains more than one interrupt value, you can assign different preemption flags to each interrupt by entering a vector of flag values to correspond to the order of the interrupts in **Interrupt numbers**. If **Interrupt numbers** contains more than one interrupt, and you enter only one flag value in this field, that status applies to all interrupts.

In the default settings [0 1], the interrupt with priority 5 in **Interrupt numbers** is not preemptible and the priority 8 interrupt can be preempted.

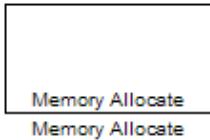
Enable simulation input

When you select this option, Simulink adds an input port to the Hardware Interrupt block. This port is used in simulation only. Connect one or more simulated interrupt sources to the simulation input.

Purpose Allocate memory section on Blackfin, SHARC, TigerSHARC processors

Library Core Support in Link for ADI VisualDSP++

Description



On your ADI processor, this block directs the VisualDSP++ compiler to allocate memory for a new variable you specify. Parameters in the block dialog box let you specify the variable name, the alignment of the variable in memory, the data type of the variable, and other features that fully define the memory required.

The block does not verify whether the entries for your variable are valid, such as checking the variable name, data type, or section. You must ensure that all variable names are valid, that they use valid data types, and that all section names you specify are valid as well.

The block does not have input or output ports. It only allocates a memory location. You do not connect it to other blocks in your model.

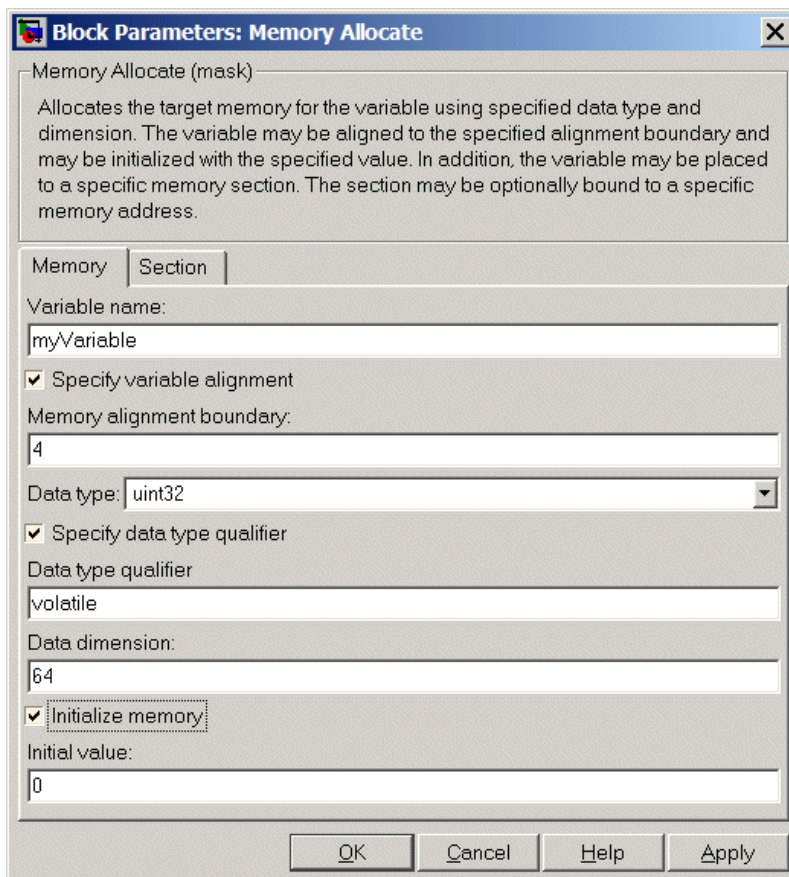
Dialog Box

The block dialog box comprises multiple tabs:

- **Memory** — Allocate the memory for storing variables. Specify the data type and size.
- **Section** — Specify the memory section in which to allocate the variable.

The dialog box images show all of the available parameters enabled. Some of the parameters shown do not appear until you select one or more other parameters.

Memory Allocate



The following sections describe the contents of each pane in the dialog box.

Memory Parameters

Block Parameters: Memory Allocate

Memory Allocate (mask)

Allocates the target memory for the variable using specified data type and dimension. The variable may be aligned to the specified alignment boundary and may be initialized with the specified value. In addition, the variable may be placed to a specific memory section. The section may be optionally bound to a specific memory address.

Memory | Section

Variable name:
myVariable

Specify variable alignment

Memory alignment boundary:
4

Data type: uint32

Specify data type qualifier

Data type qualifier
volatile

Data dimension:
64

Initialize memory

Initial value:
0

OK Cancel Help Apply

You find the following memory parameters on this tab.

Variable name

Specify the name of the variable to allocate. The variable is allocated in the generated code.

Specify variable alignment

Select this option to direct the compiler to align the variable in **Variable name** to an alignment boundary. When you select this option, the **Memory alignment boundary** parameter appears so you can specify the alignment. Use this parameter and **Memory alignment boundary** when your processor requires this feature.

Memory alignment boundary

After you select **Specify variable alignment**, this option enables you to specify the alignment boundary in bytes. If your variable contains more than one value, such as a vector or an array, the elements are aligned according to rules applied by the compiler.

Data type

Defines the data type for the variable. Select from the list of types available.

Specify data type qualifier

Selecting this enables **Data type qualifier** so you can specify the qualifier to apply to your variable.

Data type qualifier

After you select **Specify data type qualifier**, you enter the desired qualifier here. `volatile` is the default qualifier. Enter the qualifier you need as text. Common qualifiers are `static` and `register`. The block does not check for valid qualifiers.

Data dimension

Specifies the number of elements of the type you specify in **Data type**. Enter an integer here for the number of elements.

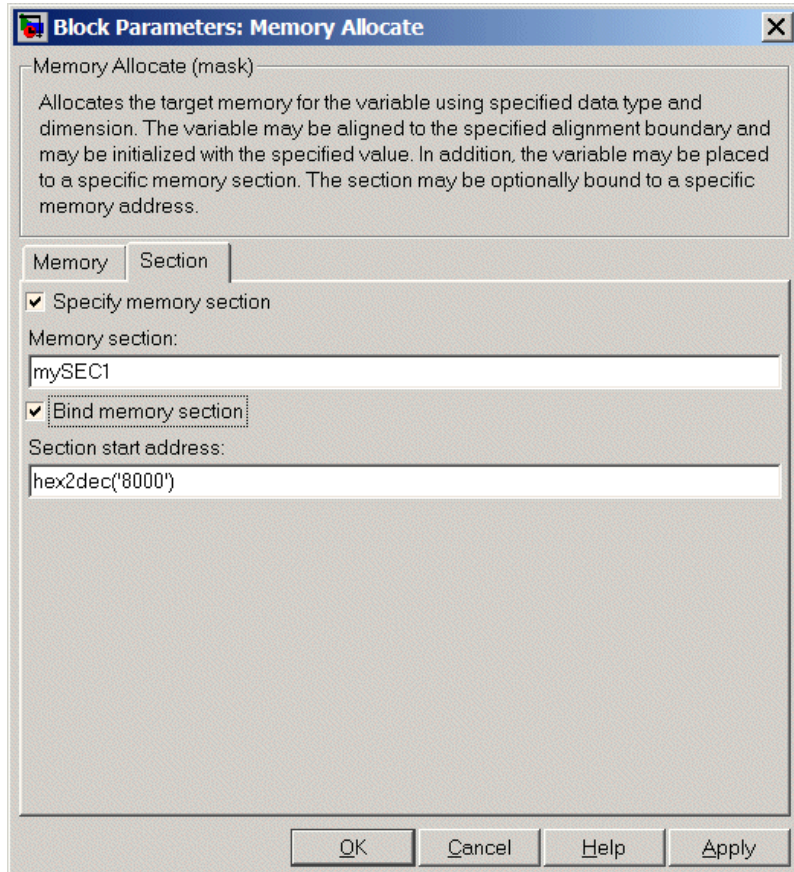
Initialize memory

Directs the block to initialize the memory location to a fixed value before processing.

Initial value

Specifies the initialization value for the variable. At run time, the block sets the memory location to this value.

Section Parameters



Parameters on this pane specify the section in memory to store the variable.

Specify memory section

Selecting this parameter enables you to specify the memory section to allocate space for the variable. Enter either one of the

Memory Allocate

standard memory sections or a custom section that you declare elsewhere in your code.

Memory section

Identify a specific memory section to allocate the variable in **Variable name**. Verify that the section has sufficient space to store your variable. After you specify a memory section by selecting **Specify memory section** and entering the section name in **Memory section**, use **Bind memory section** to bind the memory section to a location.

Bind memory section

After you specify a memory section by selecting **Specify memory section** and entering the section name in **Memory section**, use this parameter to bind the memory section to the location in memory specified in **Section start address**. When you select this, you enable the **Section start address** parameter.

The new memory section specified in **Memory section** is defined when you check this parameter.

Note Do not use **Bind memory section** for existing memory sections.

Section start address

Specify the address to which to bind the memory section. Enter the address in decimal form or in hexadecimal with a conversion to decimal as shown by the default value `hex2dec('8000')`. The block does not verify the address—verify that the address exists and can contain the memory section you entered in **Memory section**.

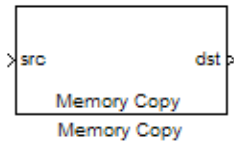
See Also

Memory Copy

Purpose Copy to and from memory section

Library Core Support in Link for ADI VisualDSP++

Description In generated code, this block copies variables or data from and to target memory as configured by the block parameters. Your model can contain as many of these blocks as you require to manipulate memory on your target.



Each block works with one variable, address, or set of addresses provided to the block. Parameters for the block let you specify both the source and destination for the memory copy, as well as options for initializing the memory locations.

Using parameters provided by the block, you can change options like the memory stride and offset at run time. In addition, by selecting various parameters in the block, you can write to memory at program initialization, at program termination, and at every sample time. The initialization process occurs once, rather than occurring for every read and write operation.

With the custom source code options, the block enables you to add custom C source code before and after each memory read and write (copy) operation. You can use the custom code capability to lock and unlock registers before and after accessing them. For example, some processors have registers that you may need to unlock and lock with EALLOW and EDIS macros before and after your program accesses them.

Block Operations

This block performs operations at three periods during program execution—initialization, real-time operations, and termination. With the options for setting memory initialization and termination, you control when and how the block initializes memory, copies to and from memory, and terminates memory operations. The parameters enable you to turn on and off memory operations in all three periods independently.

Memory Copy

Used in combination with the Memory Allocate block, this block supports building custom device drivers, such as PCI bus drivers or codec-style drivers, by letting you manipulate and allocate memory. This block does not require the Memory Allocate block to be in the model.

In a simulation, this block does not perform any operation. The block output is not defined.

Copy Memory

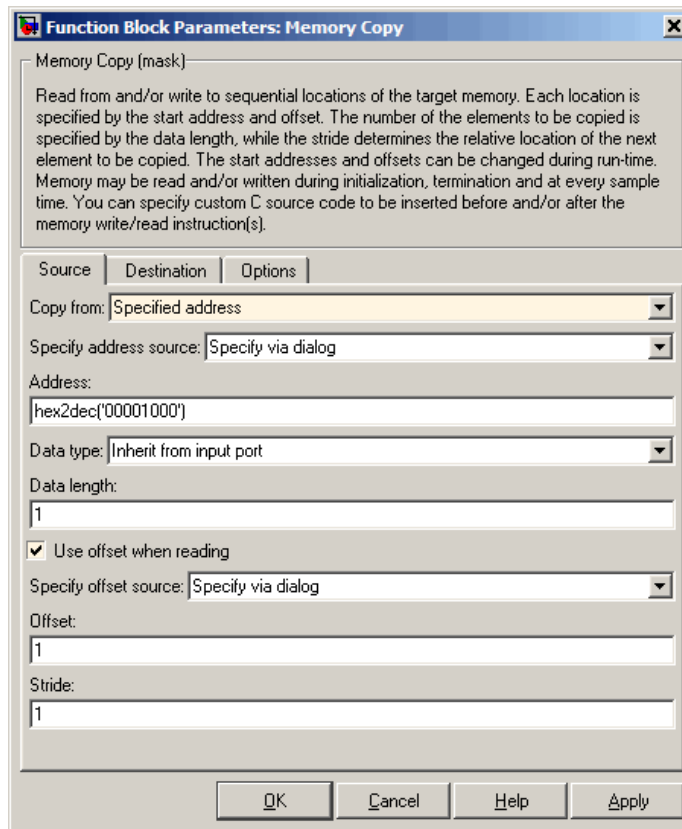
When you employ this block to copy an individual data element from the source to the destination, the block copies the element from the source in the source data type, and then casts the data element to the destination data type as provided in the block parameters.

Dialog Box

The block dialog box contains multiple tabs:

- **Source** — Identifies the sequential memory location to copy from. Specify the data type, size, and other attributes of the source variable.
- **Destination** — Specify the memory location to copy the source to. Here you also specify the attributes of the destination.
- **Options** — Select various parameters to control the copy process.

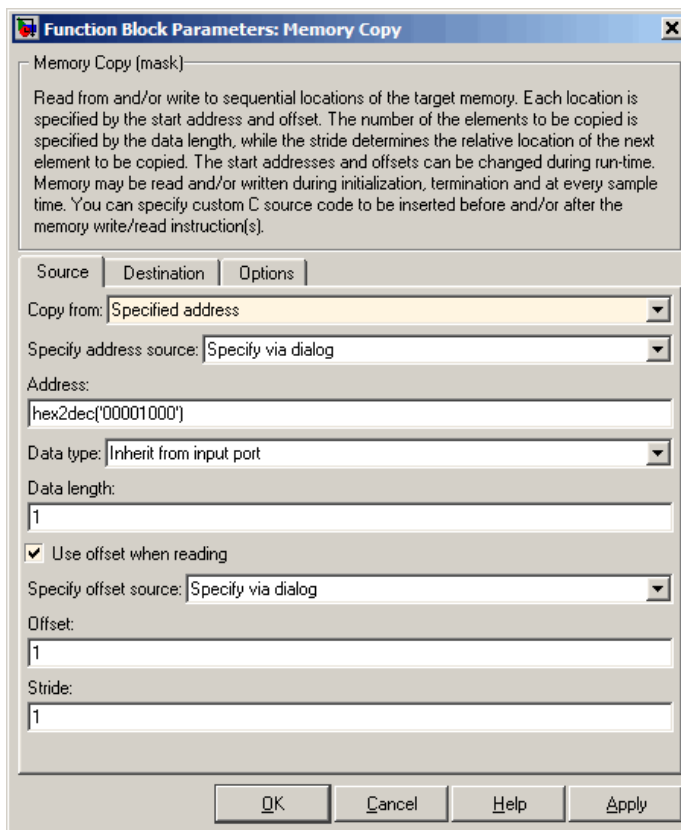
The dialog box images show many of the available parameters enabled. Some parameters shown do not appear until you select one or more other parameters. Some parameters are not shown in the figures, but the text describes them and how to make them available.



Sections that follow describe the parameters on each tab in the dialog box.

Memory Copy

Source Parameters



Copy from

Select the source of the data to copy. Choose one of the entries on the list:

- **Input port** — This source reads the data from the block input port.
- **Specified address** — This source reads the data at the specified location in **Specify address source** and **Address**.

- Specified source code symbol — This source tells the block to read the symbol (variable) you enter in **Source code symbol**. When you select this copy from option, you enable the **Source code symbol** parameter.

Note If you do not select the Input port option for **Copy from**, you must change the **Data type** parameter setting from the default Inherit from input port to one of the data types on the **Data type** list. If you do not make the change, you receive an error message that the data type cannot be inherited because the input port does not exist.

Depending on the choice you make for **Copy from**, you see other parameters that let you configure the source of the data to copy.

Specify address source

This parameter directs the block to get the address for the variable either from an entry in **Address** or from the input port to the block. Select either Specify via dialog or Input port from the list. Selecting Specify via dialog activates the **Address** parameter for you to enter the address for the variable.

When you select Input port, the port label on the block changes to &src, indicating that the block expects the address to come from the input port. Being able to change the address dynamically lets you use the block to copy different variables by providing the variable address from an upstream block in your model.

Source code symbol

Specify the symbol (variable) in the source code symbol table to copy. The symbol table for your program must include this symbol. The block does not verify that the symbol exists and uses valid syntax. Enter a string to specify the symbol exactly as you use it in your code.

Memory Copy

Address

When you select `Specify via dialog` for the address source, you enter the variable address here. Addresses should be in decimal form. Enter either the decimal address or the address as a hexadecimal string with single quotations marks and use `hex2dec` to convert the address to the proper format. The following example converts `0x1000` to decimal form.

```
4096 = hex2dec('1000');
```

For this example, you could enter either `4096` or `hex2dec('1000')` as the address.

Data type

Use this parameter to specify the type of data that your source uses. The list includes the supported data types, such as `int8`, `uint32`, and `Boolean`, and the option `Inherit` from input port for inheriting the data type for the variable from the block input port.

Data length

Specifies the number of elements to copy from the source location. Each element has the data type specified in **Data type**.

Use offset when reading

When you are reading the input, use this parameter to specify an offset for the input read. The offset value is in elements with the assigned data type. The **Specify offset source** parameter becomes available when you check this option.

Specify offset source

The block provides two sources for the offset — `Input port` and `Specify via dialog`. Selecting `Input port` configures the block input to read the offset value by adding an input port labeled `src ofs`. This port enables your program to change the offset dynamically during execution by providing the offset value as an input to the block. If you select `Specify via dialog`, you enable the **Offset** parameter in this dialog box so you can enter the offset to use when reading the input data.

Offset

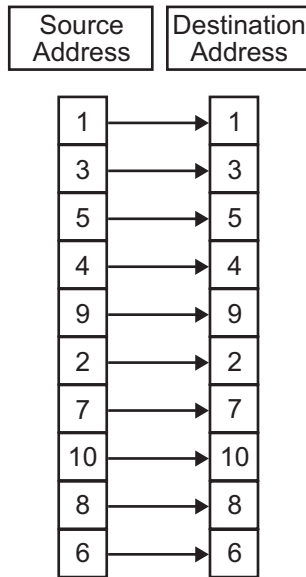
Offset tells the block whether to copy the first element of the data at the input address or value, or skip one or more values before starting to copy the input to the destination. **Offset** defines how many values to skip before copying the first value to the destination. Offset equal to one is the default value and **Offset** accepts only positive integers of one or greater.

Stride

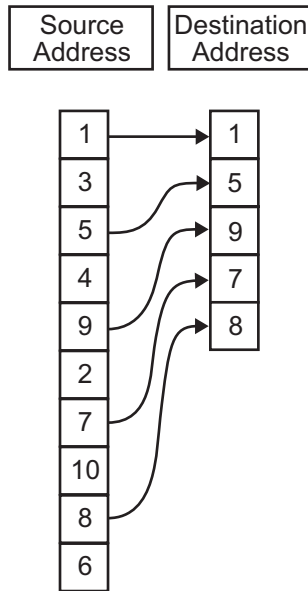
Stride lets you specify the spacing for reading the input. By default, the stride value is one, meaning the generated code reads the input data sequentially. When you add a stride value that is not equal to one, the block reads the input data elements not sequentially, but by skipping spaces in the source address equal to the stride. **Stride** must be a positive integer.

The next two figures help explain the stride concept. In the first figure you see data copied without any stride. Following that figure, the second figure shows a stride value of two applied to reading the input when the block is copying the input to an output location. You can specify a stride value for the output with parameter **Stride** on the **Destination** pane. Compare stride with offset to see the differences.

Memory Copy



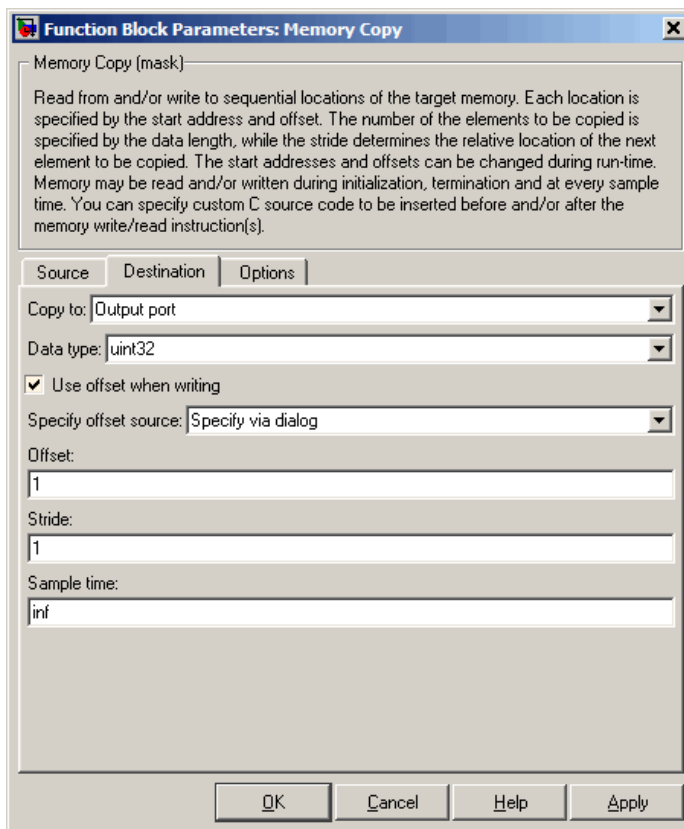
Input Stride = 1
Output Stride = 1
Number of Elements Copied = 10



Input Stride = 2
Output Stride = 1
Number of Elements Copied = 5

Memory Copy

Destination Parameters



Copy to

Select the destination for the data. Choose one of the entries on the list:

- **Output port** — Copies the data to the block output port. From the output port the block passes data to downstream blocks in the code.

- Specified address — Copies the data to the specified location in **Specify address source** and **Address**.
- Specified source code symbol — Tells the block to copy the variable or symbol (variable) to the symbol you enter in **Source code symbol**. When you select this copy to option, you enable the **Source code symbol** parameter.

Depending on the choice you make for **Copy from**, you see other parameters that let you configure the source of the data to copy.

Specify address source

This parameter directs the block to get the address for the variable either from an entry in **Address** or from the input port to the block. Select either **Specify via dialog** or **Input port** from the list. Selecting **Specify via dialog** activates the **Address** parameter for you to enter the address for the variable.

When you select **Input port**, the port label on the block changes to **&dst**, indicating that the block expects the destination address to come from the input port. Being able to change the address dynamically lets you use the block to copy different variables by providing the variable address from an upstream block in your model.

Source code symbol

Specify the symbol (variable) in the source code symbol table to copy. The symbol table for your program must include this symbol. The block does not verify that the symbol exists and uses valid syntax.

Address

When you select **Specify via dialog** for the address source, you enter the variable address here. Addresses should be in decimal form. Enter either the decimal address or the address as a hexadecimal string with single quotations marks and use **hex2dec** to convert the address to the proper format. This example converts **0x2000** to decimal form.

Memory Copy

```
8192 = hex2dec('2000');
```

For this example, you could enter either 8192 or `hex2dec('2000')` as the address.

Data type

Use this parameter to specify the type of data that your variable uses. The list includes the supported data types, such as `int8`, `uint32`, and `Boolean`, and the option `Inherit` from source for inheriting the data type for the variable from the block input port.

Specify offset source

The block provides two sources for the offset—`Input port` and `Specify via dialog`. Selecting `Input port` configures the block input to read the offset value by adding an input port labeled `src ofs`. This port enables your program to change the offset dynamically during execution by providing the offset value as an input to the block. If you select `Specify via dialog`, you enable the **Offset** parameter in this dialog box so you can enter the offset to use when writing the output data.

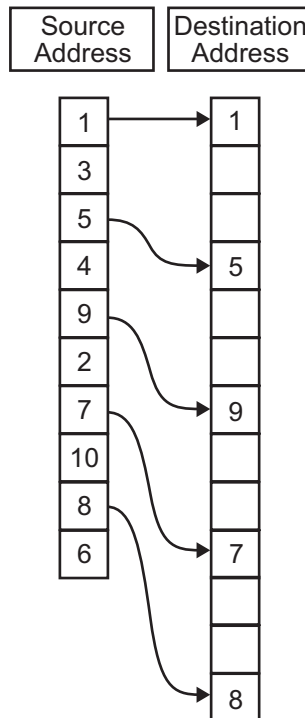
Offset

Offset tells the block whether to write the first element of the data to be copied to the first destination address location, or skip one or more locations at the destination before writing the output. **Offset** defines how many values to skip in the destination before writing the first value to the destination. One is the default offset value and **Offset** accepts only positive integers of one or greater.

Stride

Stride lets you specify the spacing for copying the input to the destination. By default, the stride value is one, meaning the generated code writes the input data sequentially to the destination in consecutive locations. When you add a stride value not equal to one, the output data is stored not sequentially, but by skipping addresses equal to the stride. **Stride** must be a positive integer.

This figure shows a stride value of three applied to writing the input to an output location. You can specify a stride value for the input with parameter **Stride** on the **Source** pane. As shown in the figure, you can use both an input stride and output stride at the same time to enable you to manipulate your memory more fully.



Input Stride = 2
Output Stride = 3
Number of Elements Copied = 5

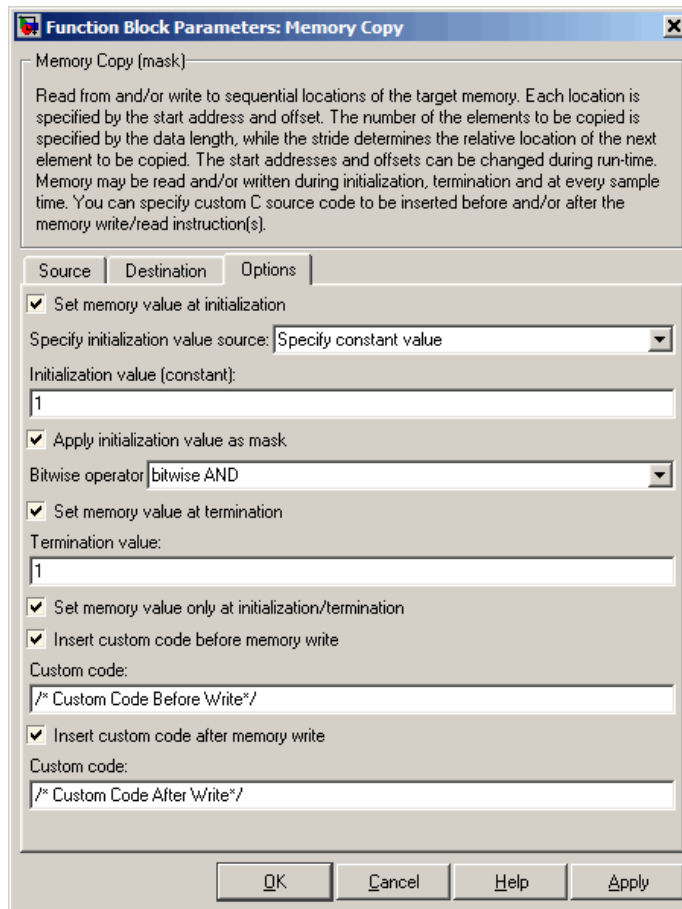
Sample time

Sample time sets the rate at which the memory copy operation occurs, in seconds. The default value `Inf` tells the block to use a

Memory Copy

constant sample time. You can set **Sample time** to -1 to direct the block to inherit the sample time from the input, if there is one, or the Simulink model (when there are no input ports on the block). Enter the sample time in seconds as you need.

Options Parameters



The image shows a dialog box titled "Function Block Parameters: Memory Copy". It has a tabbed interface with three tabs: "Source", "Destination", and "Options". The "Options" tab is currently selected. The dialog contains the following elements:

- Memory Copy (mask):** A text area containing the following description: "Read from and/or write to sequential locations of the target memory. Each location is specified by the start address and offset. The number of the elements to be copied is specified by the data length, while the stride determines the relative location of the next element to be copied. The start addresses and offsets can be changed during run-time. Memory may be read and/or written during initialization, termination and at every sample time. You can specify custom C source code to be inserted before and/or after the memory write/read instruction(s)."
- Options Tab:**
 - Set memory value at initialization
 - Specify initialization value source: Specify constant value (dropdown menu)
 - Initialization value (constant): 1 (text field)
 - Apply initialization value as mask
 - Bitwise operator: bitwise AND (dropdown menu)
 - Set memory value at termination
 - Termination value: 1 (text field)
 - Set memory value only at initialization/termination
 - Insert custom code before memory write
 - Custom code: /* Custom Code Before Write*/ (text field)
 - Insert custom code after memory write
 - Custom code: /* Custom Code After Write*/ (text field)

At the bottom of the dialog are four buttons: "OK", "Cancel", "Help", and "Apply".

Set memory value at initialization

When you check this option, you direct the block to initialize the memory location to a specific value when you initialize your program at run time. After you select this option, use the **Set memory value at termination** and **Specify initialization value source** parameters to set your desired value. Alternately, you can tell the block to get the initial value from the block input.

Specify initialization value source

After you check Set memory value at initialization, use this parameter to select the source of the initial value. Choose either

- **Specify constant value** — Sets a single value to use when your program initializes memory. Enter any value that meets your needs.
- **Specify source code symbol** — Specifies a variable (a symbol) to use for the initial value. Enter the symbol as a string.

Initialization value (constant)

If you check **Set memory value at initialization** and choose **Specify constant value** for **Specify initialization value source**, enter the constant value to use in this field. Any real value that meets your needs is acceptable.

Initialization value (source code symbol)

If you check **Set memory value at initialization** and choose **Specify source code symbol** for **Specify initialization value source**, enter the symbol to use in this field. Any symbol that meets your needs and is in the symbol table for the program is acceptable. When you enter the symbol, the block does not verify whether the symbol is a valid one. If it is not valid you get an error when you try to compile, link, and run your generated code.

Apply initialization value as mask

You can use the initialization value as a mask to manipulate register contents at the bit level. Your initialization value is treated as a string of bits for the mask.

Memory Copy

Checking this parameter enables the **Bitwise operator** parameter for you to define how to apply the mask value.

To use your initialization value as a mask, the output from the copy has to be a specific address. It cannot be an output port, but it can be a symbol.

Bitwise operator

To use the initialization value as a mask, select one of the entries on the following table from the **Bitwise operator** list to describe how to apply the value as a mask to the memory value.

Bitwise Operator List Entry	Description
bitwise AND	Apply the mask value as a bitwise AND to the value in the register.
bitwise OR	Apply the mask value as a bitwise OR to the value in the register.
bitwise exclusive OR	Apply the mask value as a bitwise exclusive OR to the value in the register.
left shift	Shift the bits in the register left by the number of bits represented by the initialization value. For example, if your initialization value is 3, the block shifts the register value to the left 3 bits. In this case, the value must be a positive integer.
right shift	Shift the bits in the register to the right by the number of bits represented by the initialization value. For example, if your initialization value is 6, the block shifts the register value to the right 6 bits. In this case, the value must be a positive integer.

Applying a mask to the copy process lets you select individual bits in the result, for example, to read the value of the fifth bit by applying the mask.

Set memory value at termination

Along with initializing memory when the program starts to access this memory location, this parameter directs the program to set memory to a specific value when the program terminates.

Set memory value only at initialization/termination

This block performs operations at three periods during program execution—initialization, real-time operations, and termination. When you check this option, the block only does the memory initialization and termination processes. It does not perform any copies during real-time operations.

Insert custom code before memory write

Select this parameter to add custom C code before the program writes to the specified memory location. When you select this option, you enable the **Custom code** parameter where you enter your C code.

Custom code

Enter the custom C code to insert into the generated code just before the memory write operation. Code you enter in this field appears in the generated code exactly as you enter it.

Insert custom code after memory write

Select this parameter to add custom C code immediately after the program writes to the specified memory location. When you select this option, you enable the **Custom code** parameter where you enter your C code.

Custom code

Enter the custom C code to insert into the generated code just after the memory write operation. Code you enter in this field appears in the generated code exactly as you enter it.

See Also

Memory Allocate

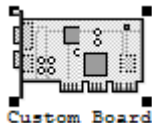
Target Preferences

Purpose

Configure model for Analog Devices processor

Library

Target Preferences in Link for Analog Devices VisualDSP++®



Description

Options on the block mask let you set features of code generation for your custom Blackfin, SHARC, or TigerSHARC processor. Adding this block to your Simulink model provides access to the processor hardware settings you need to configure when you generate code from Real-Time Workshop to run on the processor.

Any model that you target to custom hardware must include this block. Real-Time Workshop returns an error message if a target preferences block is not present in your model.

Note This block must be in your model at the top level and not in a subsystem. It does not connect to other blocks, but stands alone to set the target preferences for the model. Simulink returns an error when your model either does not include a target preferences block or has more than one.

You can specify the following processor and target options on this block:

- Board and processor information
- Memory mapping and layout
- Allocation of the various code sections, such as compiler, and custom sections

Setting the options included in this dialog box results in identifying your target to Real-Time Workshop, VisualDSP++, and Simulink, and

configuring the memory map for your target. Both steps are essential for developing code for any processor that is custom or explicitly supported.

Unlike most other blocks, you cannot open the block dialog box for this block until you add the block to a model. When you try to open the block dialog, the block attempts to connect to a VisualDSP++ session. It cannot make the connection when the block is in the library. If you try to open the block dialog before you add it to a model, the open process fails and returns an error message.

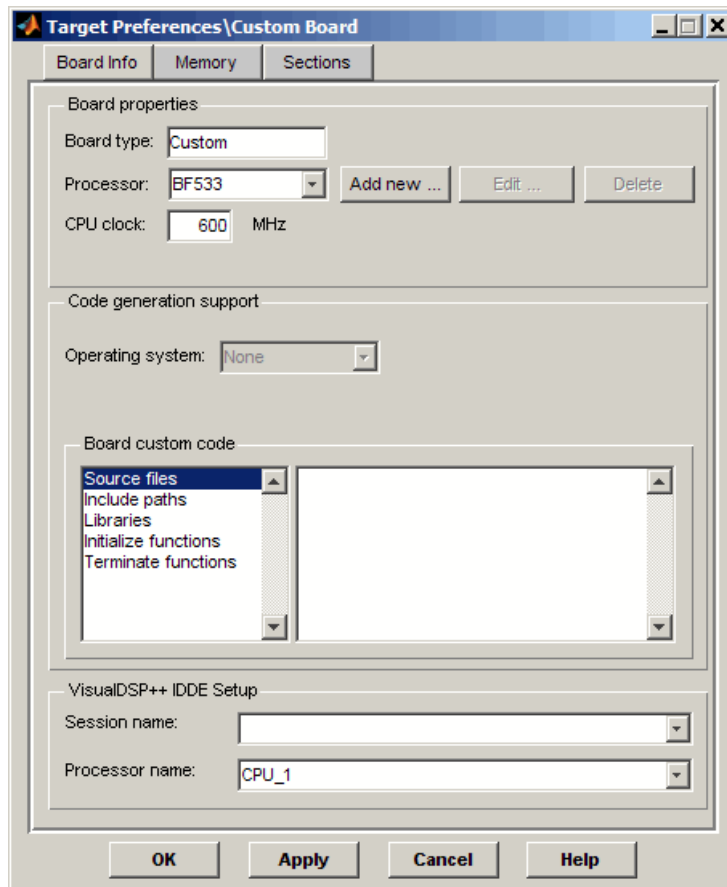
Note If you do not have VisualDSP++ installed on your PC, you cannot open this block dialog.

Generating Code from Model Subsystems

Real-Time Workshop provides the ability to generate code from a selected subsystem in a model. To generate code for an Analog Devices processor from a subsystem, the subsystem model must include this target preferences block.

Target Preferences

Dialog Box



All target preferences block dialog boxes provide tabbed access to the following panes. You set the options for the processor from these panes:

- **Board info** — Select the board type and processor, set the clock speed, and identify the session.
- **Memory** — Set the memory allocation and layout on the processor (memory mapping).

- **Sections** — Determine the arrangement and location of the sections on the processor, such as where to put the compiler information.

Board Info Pane

The following options appear on the **Board Info** pane for the **Target Preferences** dialog box.

Board Type

Enter the type of board you are targeting with the model. You can enter **Custom** to support any board, based on one of the supported processors, or enter the name of one of the supported boards.

Processor

Select the processor on the board you select in **Board type**. The processor type you enter determines the contents and setting for options on the **Memory** and **Sections** panes in this dialog box.

CPU clock

Shows the clock speed of the processor. When you enter a value, you are not changing the CPU clock rate. Instead, you are reporting the actual rate. If the value you enter does not match the rate on the processor, your model's real-time code profiling results may be incorrect.

Enter the actual clock rate the board uses. The rate you enter in this field does not change the rate on the board. Setting **CPU clock** to the actual board rate allows the code you generate to run correctly according to the actual clock rate of the hardware.

When you generate code for targets from Simulink models, you may encounter the software timer. The timer is invoked automatically to handle and create interrupts to drive your model if the processing rates in your model change (the model is multirate).

Correctly generating interrupts for your model depends on the clock rate of the CPU on your processor.

Target Preferences

For the timer software to calculate the interrupts correctly, VisualDSP++ needs to know the actual clock rate of your processor as you configured it. CPU clock speed lets you tell the timer the rate at which your processor CPU runs, which is the rate to use to match the CPU rate.

The timer uses the CPU clock rate you specify in **CPU clock** to calculate the time for each interrupt. For example, if your model includes a sine wave generator block running at 1 kHz feeding a signal into an FIR filter block, the timer needs to create interrupts to generate the sine wave samples at the proper rate. The timer uses the clock rate you enter, for example, 100 MHz, to calculate the sine generator interrupt period as follows for the sine block:

- Sine block rate = 1 kHz, or 0.001 s/sample
- CPU clock rate = 100 MHz, or 0.000000001 s/sample

To create sine block interrupts at 0.001 s/sample requires:

$$100,000,000/1000 = 1 \text{ Sine block interrupt per } 100,000 \text{ clock ticks}$$

Thus, you must report the correct clock rate, or the interrupts come at the wrong times and the results are incorrect.

Board Custom Code

Entries in this group let you specify the locations of custom source files or libraries or other functions. The following options provide access to text areas where you enter files and file paths. The block does not check whether the functions you enter are correct or the file paths you provide exist and are correct. Entering incorrect functions or paths may cause errors during code generation.

- **Source files** — Enter the full paths to source code files to use with this processor. By default, there are no entries in this parameter.

- **Include paths** — If you require additional files on your path, add them by typing the path into the text area. The default setting does not include additional paths.
- **Libraries** — These entries identify specific libraries that the processor requires. They appear on the list by default if required. Add more as you require by entering the full path to the library with the library file in the text area. No additional libraries appear in this field in the default configuration.
- **Initialize functions** — If your project requires an initialize function, enter it in this field. By default, this parameter is empty.
- **Terminate functions** — Enter a function to run when a program terminates. The default setting is not to include a specific termination function.

When you enter a path to a file, library, or other custom code, use the string

```
$(install_dir)
```

to refer to the VisualDSP++ installation directory.

Enter new paths or files (custom code items) one entry per line. Include the full path to the file for libraries and source code.

Board custom code options do not support functions that use return arguments or values. Only functions of type `void fname void` are valid as entries in these parameters.

Session name

Contains a list of all the sessions defined in VisualDSP++. From the list of available sessions, select the one to which you are targeting your code.

Processor name

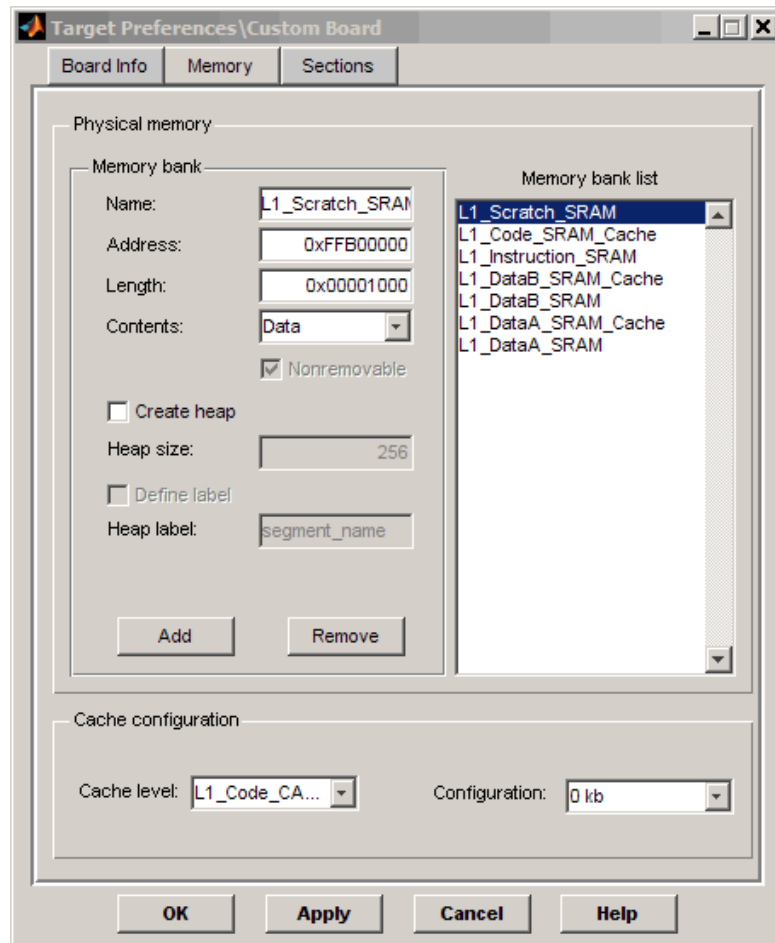
Lists the processors on the board you selected for targeting in **Session name**. In most cases, only one name appears because

Target Preferences

the board has one processor. In the multiprocessor case, you select the processor by name from the list.

Memory Pane

When you develop models for any processor, you need to specify the layout of the physical memory on your processor and board to determine how use it for your program. For supported boards, the board-specific target preferences blocks set the default memory map.



The **Memory** pane contains memory options in three areas:

- **Physical Memory** — Specify the processor and board memory map
- **Heap** — Specify whether you use a heap and determine the size in words

Target Preferences

- **Cache configuration** — Enables the cache (where available) and sets the size in kilobytes

Note Your **Physical Memory**, **Heap**, and **Cache configuration** settings on this pane may affect options on the **Sections** pane. Your choices on the **Memory** pane may change how you configure some options on the **Sections** pane.

Most of the information about memory segments and memory allocation is available from the online help system for VisualDSP++.

Physical Memory Options

This list shows the physical memory segments available on the board and processor. By default, target preferences blocks show the memory segments found on the selected processor. In addition, the **Memory** pane on preconfigured target preferences blocks shows memory segments that are available on the board, but that are external to the processor (external memory). Target preferences blocks set default starting addresses, lengths, and contents of the default memory segments.

The default memory segments for each processor and board are different. For example:

- Custom boards based on Blackfin processors provide SRAM memory segments by default.
- SHARC-based boards provide RAM memory segments by default.

Name

When you highlight an entry on the **Physical memory** list, the name of the entry appears in this field. To change the name of the existing memory segment, select it in the **Physical memory** list and then type the new name in this field.

Note You cannot change the names of default processor memory segments.

To add a new physical memory segment to the list, click **Add**, replace the temporary label in **Name** with the one to use, and press **Return**. Your new segment appears on the list.

After you add the segment, you can configure the starting address, length, and contents for the new segment. New segments start with code and data as the type of content that can be stored in the segment (refer to the **Contents** option).

Names are case sensitive. NewSegment is not the same as newsegment or newSegment.

Address

Address reports the starting address for the memory segment showing in the **Name** field. Address entries are in hexadecimal format and limited only by the board or processor memory.

When you are using a processor-specific preferences block, the starting address shown is the default value. You can change the starting value by entering the new value directly in the **Address** field when you select the memory segment to change.

Length

From the starting address, **Length** sets the length of the memory allocated to the segment in the **Name** field. As in all memory entries, specify the length in hexadecimal format, in minimum addressable data units (MADUs).

When you are using a processor-specific preferences block, the length shown is the default value. You can change the value by entering the new value directly in this option.

Target Preferences

Contents

Contents details the kind of program sections that you can store in the memory segment in **Name**. As the processor type for the target preferences block changes, the kinds of information you store in listed memory segments may change. Generally, the **Contents** list contains these strings:

- Code — Allow code to be stored in the memory segment in **Name**.
- Data — Allow data to be stored in the memory segment in **Name**.
- Code and Data — Allow code and data to be stored in the memory segment in the **Name** field. When you add a new memory segment, this string is the default setting for the contents of the new element.

You may add or use as many segments of each type as you need, within the limits of the memory on your processor.

Add

Click **Add** to add a new memory segment to the processor memory map. When you click **Add**, a new segment name appears, for example NEWMEM1, in **Name** and on the **Physical memory** list. In **Name**, change the temporary name NEWMEM1 by entering the new segment name. Entering the new name or clicking **Apply** updates the temporary name on the list to the name you enter in this field.

Remove

Remove a memory segment from the memory map. Select the segment to remove on the **Physical memory** list, and click **Remove** to delete the segment.

Memory bank list

Displays all available memory banks for the selected processor. When you select one of the entries on this list, the **Name**, **Address**, **Length**, and **Contents** parameters change to reflect the memory block selection. With the contents list, you can change the type of material stored in the block—data or code or both.

Create Heap

If your processor supports using a heap, as the Blackfin and SHARC processors do, selecting this option enables creating the heap, and enables the **Heap size** option. **Create heap** is not available on processors that either do not provide a heap or do not allow you to configure the heap.

Use this option to create a heap in any memory segment on the **Physical memory** list. Select the memory segment on the list, and then select **Create heap** to create a heap in the selected segment. After you create the heap, use the **Heap size** and **Define label** options to configure the heap.

The location of the heap in the memory segment is not under your control. The only way to control the location of the heap in a segment is to make the segment and the heap the same size. Otherwise, the compiler determines the location of the heap in the segment.

Heap Size

After you select **Create heap**, this option lets you specify the size of the heap in words. Enter the number of words in decimal format. When you enter the heap size in decimal words, the system converts the decimal value to hexadecimal format. You can enter the value directly in hexadecimal format as well. Processors may support different maximum heap sizes.

Define Label

Selecting **Create heap** enables this option that allows you to name the heap. Enter your label for the heap in the **Heap label** option.

Heap Label

Use this option which you enable by selecting **Define label**, to provide the label for the heap. Any combination of characters is accepted for the label, except reserved characters in C/C++ compilers.

Target Preferences

The block does not verify that the label you enter is valid. Invalid labels can cause errors during code generation.

Cache level

Blackfin, SHARC, and TigerSHARC processors support different cache arrangements. For Blackfin processors, you can select one of the following options from the list:

- L1_Code_CACHE
- L1_DataA_CACHE
- L1_DataB_CACHE

On SHARC processors, the cache is always Instruction_CACHE. Set the cache size in **Configuration**.

On TigerSHARC processors, the cache is always CACHE, used for both data and code, and you can only enable the cache. You cannot choose the size or configuration. Use the **Configuration** option to enable the cache.

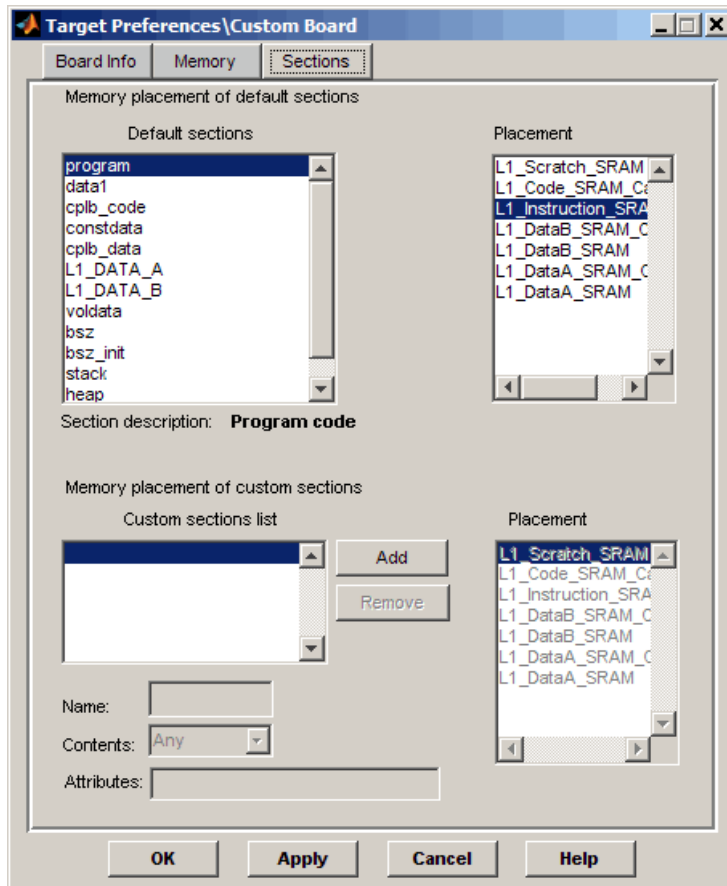
Configuration

Select the size of the cache from the list to determine the size of the cache allocated. SHARC processors support 1536 bits or 0 bits (no cache). Blackfin processors support 0 bits or 16 bits. For TigerSHARC processors, your choices are disable or enable only.

Sections Pane

Options on this pane let you specify where various program sections should go in memory. Program sections are distinct from memory segments—sections are portions of the executable code stored in contiguous memory locations. Commonly used sections include .program, .bsz, .data1, and .stack.

For more information about program sections and objects, refer to the Analog Devices VisualDSP++ online help.



Within this pane, you allocate the memory needed for the **Default sections** and **Custom sections**.

The following table provides brief definitions of the sections in the **Default sections**, and **Custom sections** lists in the pane. All sections do not appear for all processors.

Target Preferences

String	Description of the Section Contents
bsz	Global zero initialized data
bsz_init	Run-time initialization data
constdata	Constant data, usually defined with the C qualifier and string constants
cplb_code	CPLB management routines
cplb_data	CPLB configuration tables
data1	Global program data for execution
heap	System heap allocation
L1_Data_A	L1 band A SRAM data
L1_Data_B	L1 band B SRAM data
noncache_code	Code not assigned to the cache
program	Program code
seg_argv	Command line arguments that PGO uses
seg_dmda	Global data
seg_heap	System heap
seg_init	Stack and heap location and size info
seg_int_code	Interrupt latch register modifier code
seg_pmco	Program code
seg_pmda	Global program data qualified with pm keyword
seg_rth	Interrupt vector table
seg_stak	System stack
stack	Global system stack
voldata	Volatile data

You can learn more about memory sections and objects in your Analog Devices VisualDSP++ online help.

Default sections

During program compilation, the compiler produces both uninitialized and initialized blocks of data and code. These blocks get allocated into memory as required by the configuration of your system. On the **Default sections** list you find both initialized sections that contain data or executable code and uninitialized sections that reserve space in memory.

The following sections are initialized:

- bsz
- bsz_init
- constdata
- seg_pmco
- seg_pmda
- voldata (created by the assembler)

The following sections are not initialized:

- (created by the assembler)
- heap
- stack
-

The following sections appear on the list as well:

- (created by the assembler)
-
-

Note The C/C++ compiler does not use the .data section.

Target Preferences

When you highlight a section on the list, **Section description** shows a brief description of the section. Also, **Placement** shows you where the section is presently allocated in memory.

Section description

Describes the contents of the selected entry on the **Default sections** list.

Placement

Shows you where the selected **Default sections** list entry is allocated in memory. You change the memory allocation by selecting a different location from the **Placement** list. The list contains the memory segments as defined in the physical memory map on the **Memory** pane. Select one of the listed memory segments to allocate the highlighted compiler section to the segment.

Custom sections list

When your program uses code or data sections that are not included in the **Default sections** list, add the new sections to this list. Initially, the **Custom sections list** parameter contains no fixed entries. Only a placeholder for a section for you to define.

Name

Enter the name for your new section in this field. To add a new section, click **Add**. Then, replace the temporary name with the name to use. Although the temporary name includes a period at the beginning you do not need to include a period in your new name. Names are case sensitive. `NewSection` is not the same as `newsection`, or `newSection`.

Contents

Select the kind of data to assign to the new section. Choose from one of the following list entries:

- Any — Indicates the section can store either code or data. New sections use Any by default.
- Code — Indicates the section stores code.
- Data — Indicates the section stores data.

Attributes

TBD

Placement

After you have added the new section to the **Name** list, select the memory segment to which to add your new section. Limited only by the restrictions imposed by the hardware and compiler, you can select any segment that appears on the list.

Add

Click **Add** to add a new entry on the list of custom sections. When you click **Add**, a new temporary name, for example NEWMEM1 appears in the **Name** field. Enter the new custom section name to add the section to the **Custom sections** list. After you enter the new name, click **Apply** to add the new section to the list. You can also click **OK** to add the section to the list and close the dialog box.

Remove

Remove a section from the **Custom sections** list. To remove a section, select the section, and click **Remove**.

New Processor Dialog Box

Clicking **Add new** on the **General** pane opens this dialog box to add a new processor to the list of supported processors. The new processor must be a member of one of the supported families of processors.

The first time you click **Save** to add a new processor definition to the list of supported processors, a dialog box opens that directs you to select a destination folder for the saved processor definitions file customChipInfo.dat. You must select a directory to which you have write access. The location you specify becomes part of your MATLAB preferences. Future processors that you add become entries in the file customChipInfo.dat.

To add a new processor, enter values for the following parameters:

Target Preferences

Name

Provide a name to identify your new processor. You can use any valid C string value in this field. The name you enter in this field appears on the list of processors after you add the new processor.

Processor Class

Identifies the class of the new processor. Your new processor must be a member of a family of processors that Link for ADI VisualDSP++ supports. For example, you can add a new Blackfin processor because the product support the Blackfin processor family.

CPU clock

Provide a name to identify your new processor. You can use any valid C string value in this field. The name you enter in this field appears on the list of processors after you add the new processor.

Enter the clock speed of the processor in MHz. When you enter a value, you are not setting the CPU clock rate on the processor. You are reporting the rate. If the value you enter does not match the rate on the processor, your model's real-time results may be wrong, and code profiling results are not correct.

Setting **CPU clock** to the actual board rate allows the generated code to run correctly according to the actual clock rate of the hardware.

Compiler switch

This string ensures that the compile operation works successfully.

Code generation hook

This string provides the prefix that the calling code uses to call hook functions during code generation.

Define internal memory banks (one or more memory banks)

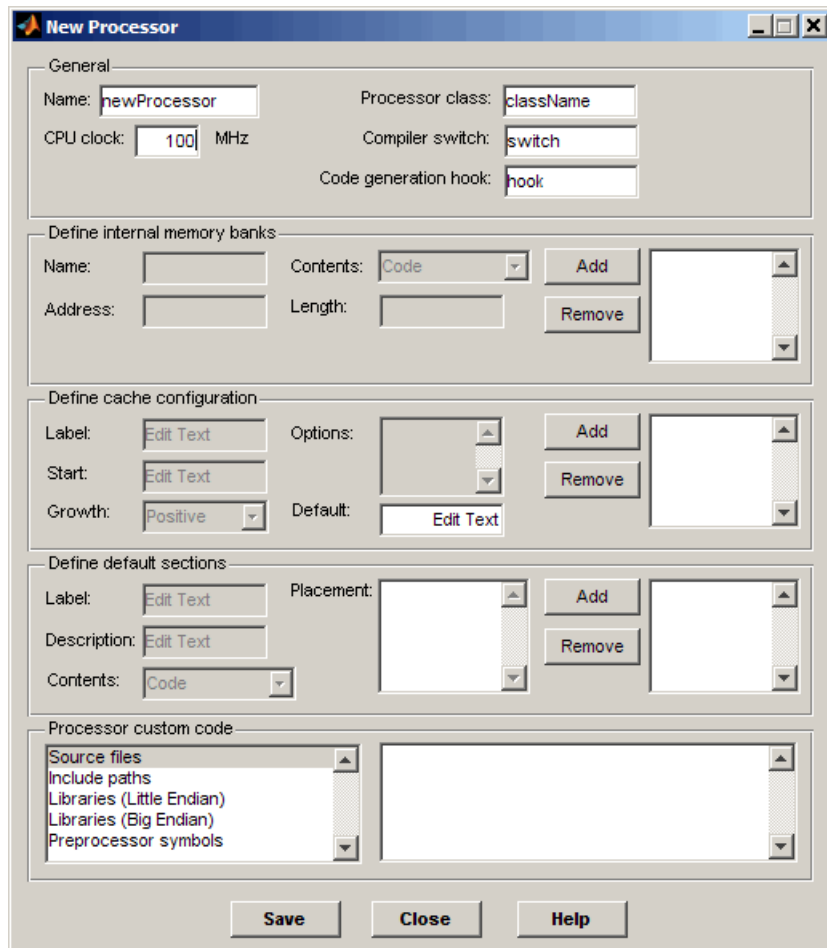
Parameters in this group configure the memory map for the new processor.

Define default sections (one or more default sections)

Parameters in this group configure the default sections for your new processor.

If you do not provide an entry for each of these parameters, Link for ADI VisualDSP++ returns an error message and does not create the new processor entry.

Target Preferences



General

Name

Provide a name to identify your new processor. You can use any valid C string in this field. The name you enter appears on the list of processors after you add the new processor.

CPU clock

Enter the clock speed of the processor in MHz. When you enter a value, you are not setting the CPU clock rate on the processor. You are reporting the rate. If the value you enter does not match the rate on the processor, your model's real-time results and code profiling results may not be correct.

Setting **CPU clock** to the actual board rate allows the code you generate to run correctly according to the actual clock rate of the hardware.

Processor class

This represents the class for the new processor. New processors must be members of processor families that Link for ADI VisualDSP++ supports, such as a new Blackfin processor or a new TigerSHARC processor.

Generally, processors in a family share common design elements such as interrupt architecture and clock. They may have different memory maps. By selecting the processor class, you identify the common features of the processor family. The parameters in **Define internal memory banks** and **Define default sections** enable you to specify the memory mapping for your new processor.

For example, to add a new Blackfin processor, enter the string TBD.

The following table shows the strings for the supported processor families.

Processor Family	Processor Class String
Blackfin	
SHARC	
TigerSHARC	

Target Preferences

Compiler switch

Identifies the processor family of the new processor to the compiler. Successful compilation requires this switch. The string depends on the processor family or class. For example, to set the compiler switch for a new SHARC processor, enter TBD.

The compiler switch strings for the supported processors appear in the following table.

Processor Class or Family	Compiler Switch String
Blackfin	
SHARC	
TigerSHARC	

Code generation hook

This string represents a prefix to add when the code generation process call certain hook functions. The hook allows the code to call into handling functions that are specific to the processor selected.

The code generation hook strings for the supported processors appear in the following table.

Processor Class or Family	Code Generation Hook String
Blackfin	
SHARC	
TigerSHARC	

Define internal memory banks

Name

To add a new physical memory segment to the internal memory banks list, click **Add**, replace the temporary label in **Name** with

the one to use, and press **Return**. Your new segment appears on the list.

After you add the segment, you can configure the starting address, length, and contents for the new segment. New segments start with code and data as the type of content that can be stored in the segment (refer to the **Contents** option).

Names are case sensitive. NewSegment is not the same as newsegment or newSegment.

Address

Address reports the starting address in hexadecimal format for the memory segment showing in **Name**. Address entries are limited only by the board or processor memory.

When you are using a processor-specific preferences block, the starting address shown is the default value. You can change the starting value by entering the new value directly in **Address** when you select the memory segment to change.

Length

From the starting address, **Length** sets the length of the memory allocated to the segment in **Name**. As in all memory entries, specify the length in hexadecimal format, in minimum addressable data units (MADUs). For the Analog Devices processor families, for example, the MADU is 8 bytes, 1 word.

Contents

Contents specifies the kind of program sections that you can store in the memory segment in **Name**. When you change the processor type, the kinds of information you can store in listed memory segments may change. Generally, the **Contents** list contains these strings:

- Code — Allow code to be stored in the memory segment in **Name**.

Target Preferences

- **Data** — Allow data to be stored in the memory segment in **Name**.
- **Code and Data** — Allow code and data to be stored in the memory segment in **Name**. When you add a new memory segment, this setting is the default for the contents of the new element.

You may add or use as many segments of each type as you need, within the limits of the memory on your processor.

Add

Click **Add** to add a new memory segment to the processor memory map. When you click **Add**, a new segment name appears, for example NEWMEM1, in **Name** and on the list. In **Name**, change the temporary name NEWMEM1 by entering the new segment name. Entering the new name, or clicking **OK** updates the temporary name on the list to the name you enter.

Remove

Remove a memory segment from the memory map. Select the segment to remove from the list, and click **Remove** to delete the segment.

Define cache configuration

Options

Enter the label for each option of the selected cache configuration, one label on each line, such as 0kb, 16kb, 32kb and so on.

Add

Click **Add** to add a new cache configuration to the list. When you click **Add**, the new cache label appears on the list.

Remove

Remove a cache configuration from the cache list. Select the configuration to remove from the list, and click **Remove** to delete the cache.

Cache configurations and related options are defined as symbols to the project generator component. Cache options for new processors are not labeled until you add the labels.

Label

Enter your label for the heap in the **Label** field. Entering the label updates the label of the selected configuration.

Define Default Sections

Options in this region let you specify where various program sections go in memory and the contents and label for each section. You can add text to describe each section. Program sections are distinct from memory segments—sections are portions of the executable code stored in contiguous memory locations. Commonly used sections include `.text`, `.bss`, `.data`, and `.stack`. Some sections relate to the compiler, and some can be custom sections as you require.

Label

The name of the section corresponds to the symbolic name recognized by the linker program used with the respective processor.

Contents

Contents provides the information about the native of the program section. As the processor type for the target preferences block changes, the kinds of information you store in listed sections may change. Generally, the **Contents** list contains these strings:

- Code — Allow code to be stored in the section in **Name**.
- Data — Allow data to be stored in the section in **Name**.
- Code and Data — Allow code and data to be stored in the section in **Name**. When you add a new section, this setting is the default for the contents.

You may add or use as many sections of each type as you need, within the limits of the memory on your processor.

Target Preferences

Add

Click **Add** to add a new section to the list. When you click **Add**, the new section appears on the list.

Remove

This option lets you remove a section from the section list. Select the section to remove from the list, and click **Remove** to delete the section.

Sections and related options are defined as symbols to the project generator component. Section options for new processors are not labeled until you add the labels.

Processor Custom Code

The list on the left side of the pane shows the kinds of custom code you can specify for your processor. Each time you use your custom processor as defined in this dialog box, the custom code you enter in this field applies. You can enter custom code in the categories in the following table.

Custom Code Entry	Description
Source files	Enter the full paths to source code files to use with this processor. By default there are no entries in this parameter. Enter each source file on a new line.
Include paths	If you require additional header files on your path, add them by typing the path into the text area, one file per line. The default setting does not include additional paths.
Libraries (Little Endian)	These entries identify specific little endian libraries that the processor requires. Add more as you require by entering the full path to the library with the library file in the text area. Enter one library per line. No additional libraries appear in the default configuration.

Custom Code Entry	Description
Libraries (Big Endian)	These entries identify specific big endian libraries that the processor requires. Add more as you require by entering the full path to the library with the library file in the text area. No additional libraries appear in the default configuration. Enter one library per line.
Preprocessor symbols	Enter any preprocessor symbols that the new processor requires for operation and compilation. No preprocessor symbols appear in the default configuration. Add the required symbols one symbol per line.

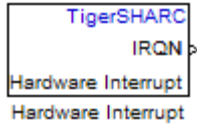
You can use two types of tokens when you specify custom code paths:

- `$(Install_dir)` — Refers to the installation directory of VisualDSP++. One example of this token is
`$(Install_dir) \vdsplink\csl\lib\...`
- `$(MATLAB_ROOT)` — Refers to the directory where you installed MATLAB.

TigerSHARC Hardware Interrupt

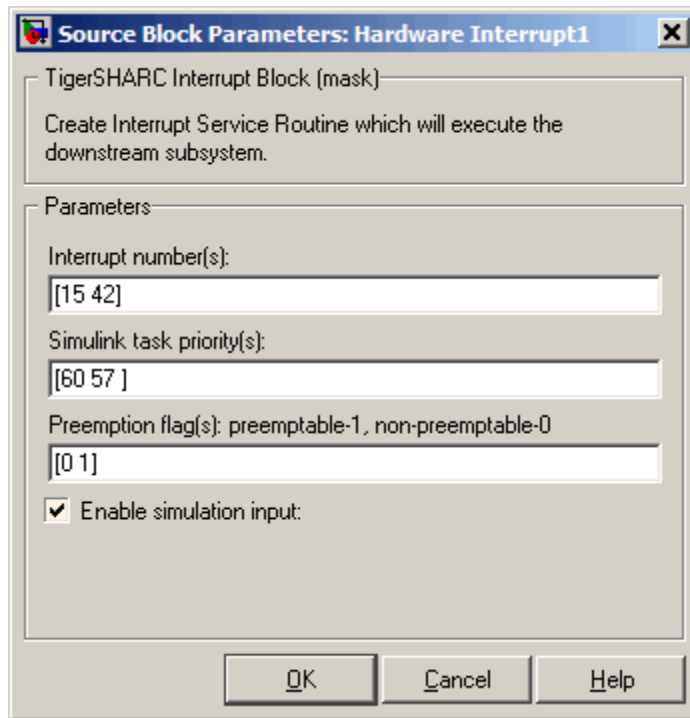
Purpose Generate Interrupt Service Routine

Library TigerSHARC DSP Support in Link for Analog Devices VisualDSP++®



Description Create interrupt service routines (ISR) in the software generated by the build process. When you incorporate this block in your model, code generation results in ISRs on the processor that run the processes that are downstream from the this block or an Idle Task block connected to this block.

Dialog Box



Interrupt number(s)

Specify an array of interrupt numbers for the interrupts to install. The valid range is 1 to 15.

The width of the block output signal corresponds to the number of interrupt numbers specified in this field. Combined with the **Simulink task priority(s)** that you enter and the preemption flag you enter for each interrupt, these three values define how the code and processor handle interrupts during asynchronous scheduler operations.

Simulink task priority(s)

Each output of the Hardware Interrupt block drives a downstream block (for example, a function call subsystem). Simulink task

priority specifies the Simulink priority of the downstream blocks. Specify an array of priorities corresponding to the interrupt numbers entered in **Interrupt number(s)**.

Simulink task priority values are required to generate the proper rate transition code (see Rate Transitions and Asynchronous Blocks). The task priority values are also required to ensure absolute time integrity when the asynchronous task needs to obtain real time from its base rate or its caller. Typically, you assign priorities for these asynchronous tasks that are higher than the priorities assigned to periodic tasks.

Preemption flag(s) preemptable – 1, non-preemptable – 0

Higher priority interrupts can preempt interrupts that have lower priority. To allow you to control preemption, use the preemption flags to specify whether an interrupt can be preempted.

Entering 1 indicates that the interrupt can be preempted. Entering 0 indicates the interrupt cannot be preempted. When **Interrupt numbers** contains more than one interrupt priority, you can assign different preemption flags to each interrupt by entering a vector of flag values, corresponding to the order of the interrupts in **Interrupt numbers**. If **Interrupt numbers** contains more than one interrupt, and you enter only one flag value in this field, that status applies to all interrupts.

In the default settings [0 1], the interrupt with priority 5 in **Interrupt numbers** is not preemptible and the priority 8 interrupt can be preempted.

Enable simulation input

When you select this option, Simulink adds an input port to the Hardware Interrupt block. This port is used in simulation only. Connect one or more simulated interrupt sources to the simulation input.

Examples

Use this list to find examples in the documentation.

Automation Interface

“Getting Started with Automation Interface” on page 2-2

Working with Links

“Example — Constructor for adivdsp Objects” on page 2-13

“Example — Setting Link Property Values at Construction” on page 2-16

“Example — Setting Link Property Values Using set” on page 2-17

“Example — Retrieving Link Property Values Using get” on page 2-17

“Example — Direct Property Referencing in Links” on page 2-17

Asynchronous Scheduler

“Asynchronous Scheduler Examples” on page 3-12

“Idle Task” on page 3-15

“Hardware Interrupt Triggered Task” on page 3-16

Project Generator

“Project Generator Tutorial” on page 3-17

Verification

“PIL Block” on page 4-6

“Real-Time Execution Profiling” on page 4-9

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